



WC7220B0 Datasheet

Standalone Bluetooth 4.1 (single mode BLE) module with
integrated chip antenna

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Revision History:

Revision	Revision Date	Originator	Changes
0.03	26/12/2016	SA	Initial version Datasheet
1.03	06/06/2017	Suresh	Format change

1. General Description

This specification provides general information regarding the performance and integration of WC7220B0, a complete wireless subsystem featuring Bluetooth Low Energy (BLE) capabilities in a small form factor module. The WC7220B0 device is designed to simplify the process of adding wireless capability without lengthy design cycles or complex RF design. Highly integrated module enables quick time to market. WC7220B0 has been fully optimized for throughput and receive sensitivity using careful design practices. Module offers resources to the customer to develop their unique software applications without requiring an external microcontroller.

1.1 Bluetooth Features

- Bluetooth® v4.1 specification compliant
- Standalone single mode Bluetooth v4.1/BLE
- Bluetooth Smart
- 128KB memory: 64KB RAM and 64KB ROM
- 512Kb EEPROM for firmware, Application code and MAC addresses storage
- RSSI monitoring for proximity applications
- <900nA current consumption in dormant mode
- 32kHz and 16MHz crystal or system clock
- Switch-mode power supply
- Programmable general purpose PIO controller
- 10-bit ADC and a DAC
- 12 digital PIOs and 1 analogue AIO
- UART
- I²C for EEPROM and peripherals
- Debug SPI
- 4 PWM modules
- Size: 8 x 12 x 1.86 mm
- Extended Temperature -30 to 85 0C
- Wake-up interrupt and watchdog timer

1.2 Bluetooth Stack

Protocol stack runs on the integrated MCU

- Bluetooth v4.1 specification features
 - Master and slave operation
 - Including encryption
- Software stack in firmware includes

- GAP
- L2CAP
- Security manager
- Attribute protocol
- Attribute profile
- Bluetooth low energy profile support

1.3 Auxiliary Features

- Battery monitor
- Power management features include software shutdown and hardware wake-up
- Power-on-reset cell detects low supply voltage
- WC7220B0 can run in low power modes from an external 32.768kHz clock signal
- Power-on-reset cell detects low supply voltage

2. System Description

WC7220B0 module is a subsystem and by itself and all the components needed to operate the radio which includes Bluetooth Baseband, MAC and RF, crystals, Filter, Antenna, Integrated MCU, Integrated SMPS, Power Amplifier, memory for the stack and for the user applications.

2.1 Block Diagram

Block diagram of WC7220B0 along with the interfaces.

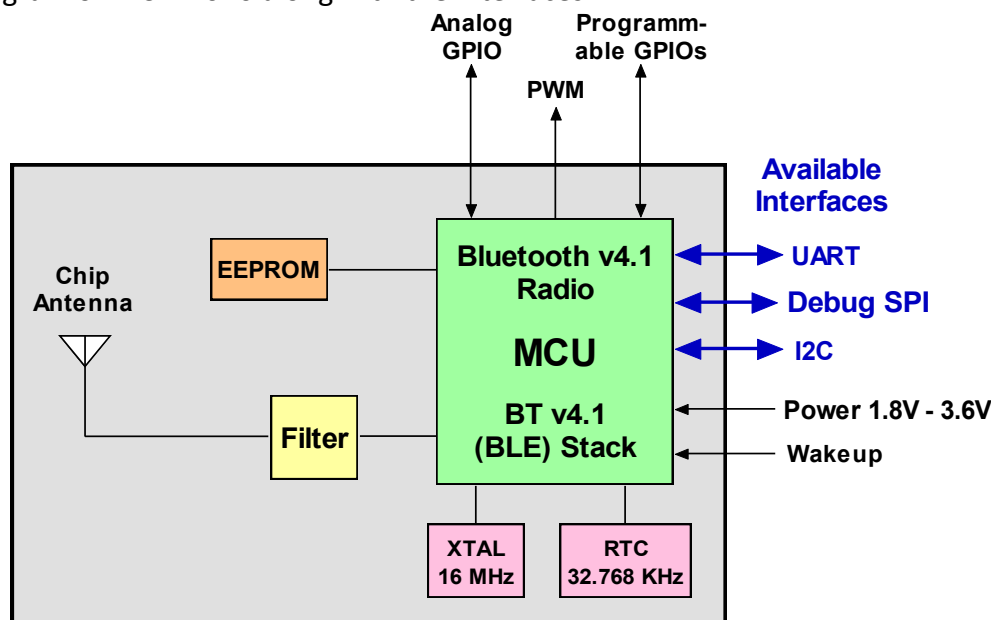


Figure 1 : Block Diagram

2.2 Pin Diagram and Description

Figure 2 shows the pin assignments for the 32-pin package

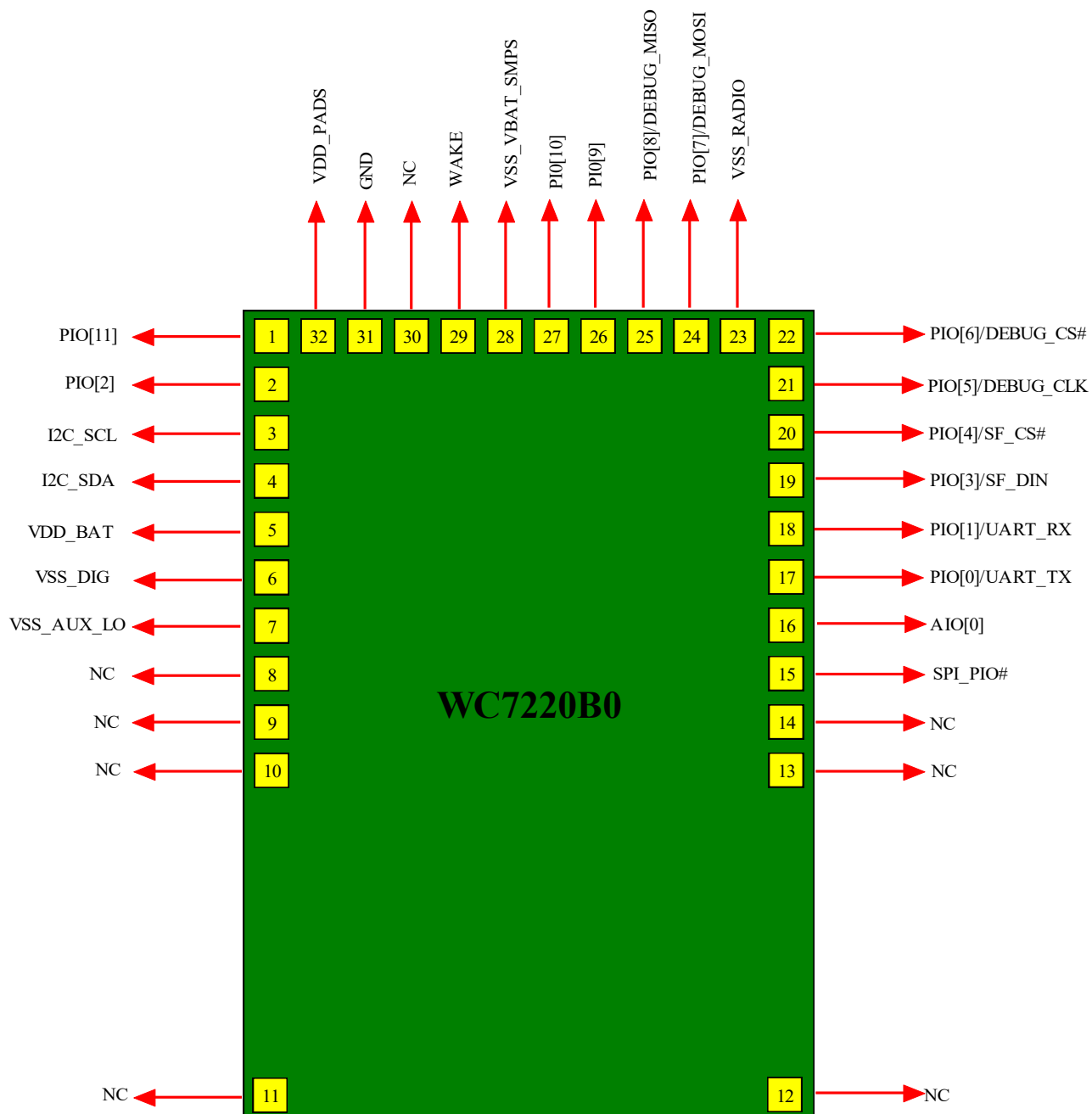


Figure 2: Pin Diagram

2.3 Physical Dimensions and Pad Locations

- Module Physical Size: 8 x 12 x 1.86 mm (including shield)
- Solder Pad Size: 0.35 x 0.35 mm
- Pad Pitch: 0.65 mm
- Pad Finish: ENIG (Electro-less Nickel Immersion Gold)
- Pads: 32

 Note: For Hardware Application notes, module dimensions and symbol library files, contact Wi2Wi sales or send an email to sales@wi2wi.com

2.4 Pin Description

Pin No	Pin Name	Type	Supply	Description
PIO_PORT				
17	PIO[0] /UART_TX	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line or UART TX to external device.
18	PIO[1] /UART_RX	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line or UART RX from external device.
2	PIO[2]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	No Connect
19	PIO[3]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line SF_DIN ¹
20	PIO[4]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line SF_CS# ¹
26	PIO[9]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line.
27	PIO[10]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line.

1	PIO[11]	Bidirectional with programmable strength internal pullup/down	VDD_PADS	Programmable I/O line.
16	AIO[0]	Bidirectional analogue	VDD_AUX 1.35V Internally generated	Analogue programmable I/O line.
Interface Signals				
3	I2C_SCL	Input with weak internal pull-up	VDD_PADS	I ² C clock
4	I2C_SDA	Bidirectional, tristate, with weak Internal Pullup	VDD_PADS	I ² C data input / output
Test and Debug				
15	SPI_PIO#	Input with strong internal pull-down	VDD_PADS	Selects SPI debug on PIO[8:5]
25	PIO[8] / DEBUG_MISO	Bidirectional with programmable strength internal pullup/ down	VDD_PADS	Programmable I/O line or debug SPI MISO selected by SPI_PIO#.
24	PIO[7] / DEBUG_MOSI	Bidirectional with programmable strength internal pullup/ down	VDD_PADS	Programmable I/O line or debug SPI MOSI selected by SPI_PIO#.
22	PIO[6] / DEBUG_CS#	Bidirectional with programmable strength internal pullup/ down	VDD_PADS	Programmable I/O line or debug SPI chip select (CS#) selected by SPI_PIO#.
21	PIO[5] / DEBUG_CLK	Bidirectional with programmable strength internal pullup/ down	VDD_PADS	Programmable I/O line or debug SPI CLK selected by SPI_PIO#.
Wake-up				
29	WAKE	Input has no internal pull-up or pull-down, use external pulldown.	VDD_BAT	Input to wake WC7220B0 from hibernate or dormant.

Power Supplies and Control				
5	VDD_BAT	Power Supply	Power Supply	Positive supply for digital domain, Input Voltage to the internal Switcher
32	VDD_PADS	Power Supply	Power Supply	Positive supply for all digital I/O ports PIO[11:0]
Ground				
23	VSS_RADIO	RF Ground	GND	RF Ground
28	VSS_BAT_SMPS	Switcher Ground	GND	Switcher Ground
6	VSS_DIG	Digital Ground	GND	Digital Ground
31	GND	GND	GND	GND
7	VSS_AUX_LO	Analog Ground	GND	Analog Ground
No Connect				
8	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
9	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
10	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
11	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
12	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
13	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
14	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating
30	NC	No Connect	No Connect	Do not Connect, Leave this pin Floating

Table 1: Pin Description Table

 ¹ Note these functions are not available with the current release.

3. Electrical Characteristics

3.1 Absolute Maximum Ratings

Rating	Min	Max	Units
Storage Temp	-40	85	°C
Battery (VDD_BAT) operation	1.8	4.4	V
I/O supply voltage	-0.4	4.4	V
Other terminal voltages(a)	VSS - 0.4	VDD + 0.4	V

Table 2: Absolute Maximum Ratings

3.2 Recommended Operating Conditions

Operating Condition	Min	Typ	Max	Unit
Operating temperature range	-30	-	85	°C
Battery (VDD_BAT) operation	1.8	-	3.6	V
I/O supply voltage (VDD_PADS)	1.2	-	3.6	V

Table 3: Recommended Operating Conditions

3.3 Power Supply

Power Supply	Min	Typ	Max	Unit
Input voltage	1.8	3.3	3.6	V

Table 4: Power Supply

3.4 Digital Terminals

Input Voltage Levels	Min	Typ	Max	Unit
VIL input logic level low	-0.4	-	0.3 x VDD_PADS	V
VIH input logic level high	0.7 x VDD_PADS	-	VDD_PADS + 0.4	V
Tr/Tf	-	-	25	nS
Output Voltage Levels	Min	Typ	Max	Unit
VOL output logic level low, IOL = 4.0mA	-	-	0.4	V
VOH output logic level high, IOH = -4.0mA	0.75 x VDD_PADS	-	-	V
Tr/Tf	-	-	5ms	ns

Table 5 : Logic Levels

Input, Output and Tristate Currents(a)	Min	Typ	Max	Unit
IOL output current low, VOL max	-	8	10	mA
IOH output current high, VOH min	-	8	10	mA
With strong pull-up	-150	-40	-10	uA
I ² C with strong pull-up	250	-	-	uA
With strong pull-down	10	40	150	uA
With weak pull-up	-5	-1	-0.33	uA
With weak pull-down	0.33	1	5	uA
CI input capacitance	1	-	5	pF

Table 6 : Digital Terminals

3.5 Analog I/O

Input/Output Voltage Levels	Min	Typ	Max	Unit
Input voltage	0	-	1.35	V
Output voltage	0	-	1.35	V
Output drive strength	-	4		mA

Table 7: Analog I/O

3.6 Auxiliary ADC

Auxiliary ADC		Min	Typ	Max	Unit
Resolution		-	-	10	bits
Input voltage range(a)		0	-	1.35	V
Accuracy	INL	-3	-	3	LSB
	DNL	-3	-	3	LSB
Offset		-1	-	1	LSB
Gain error		-0.8	-	0.8	%
Input bandwidth		-	100	-	KHz
Conversion time (measured at application)			46		uS
Sample rate(b)				21000	samples/S
ADC block conversion current			410		uA

Table 8: Auxiliary ADC



Note: (a): LSB size = VDD_AUX/1023

(b): The auxiliary ADC is accessed through the firmware API.

The sample rate given is achieved as part of this function.

3.7 Auxiliary DAC

Auxiliary DAC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Analog Supply Voltage	1.3	1.35	1.4	V
Output voltage range	0	-	1.35	V
Full-scale output voltage	1.3	1.35	1.4	V
LSB size	0	1.32	2.64	mV
Offset	-1.32	0	1.32	mV
Integral non-linearity	-3	0	3	LSB
Settling time	-	-	250	nS

Table 9: Auxiliary DAC



Note: Access to the auxiliary DAC is firmware-dependent, for more information about its availability contact Wi2Wi.

3.8 ESD Protection

Apply ESD static handling precautions during manufacturing.

Condition	Class	Max Rating
Charged Device Model Contact Discharge per JEDEC EIA/JESD22-C101	C2	1000V (all pins)

Table 10: Electrical Characteristics

4. BLE Power-Save Modes

Three types of power save modes are available in WC7220B0. They are Deep Sleep mode, Hibernate mode, and dormant mode. The key difference between the three modes is the current consumption, and the time it takes for the transition between the power save mode and normal BLE operation.

4.1 Deep Sleep

In Deep Sleep mode, the VDD_PADS and VDD_BAT domains are powered, the sleep clock is ON but the reference clock is OFF, the RAM is ON, the digital circuits are ON and the SMPS is ON (low-power mode). There is a configurable wake-up time. WC7220B0 is woken from Deep Sleep mode by any PIO configured to wake the IC.

4.2 Hibernate Mode

In Hibernate mode, the VDD_PADS and VDD_BAT domains are powered and the sleep clock is ON. The reference clock is OFF. WC7220B0 is woken from Hibernate mode by a selected level on the WAKE pin or by the watchdog timer. When requesting Hibernate, a non-zero duration must be provided. This will be added onto the current system time to calculate the next wakeup time. The device will automatically wake up after the time has passed, or sooner if there is an external wake event on the dedicated WAKE pin. Hibernate duration is expressed in microseconds.

4.3 Dormant Mode

In this mode WC7220B0 will wake up for an external event otherwise which is same as Hibernate mode.

5. Serial Interface

5.1 UART Interface

The WC7220B0 UART interface provides a simple mechanism for communicating with other serial devices using the RS232 protocol. 2 signals implement the UART function, UART_TX and UART_RX. When WC7220B0 is connected to another digital device, UART_RX and UART_TX transfer data between the 2 devices. UART configuration parameters, e.g. baud rate and data format, are set using WC7220B0 firmware.

When selected in firmware PIO[0] is assigned to a UART_TX output and PIO[1] is assigned to a UART_RX input, The details are provided in the Table 1: Pin Description Table.

UART Parameters

Minimum Baud rate Supported are: 2400 baud with < 2% Error rate
: 9600 baud with < 2% Error rate

Maximum Baud rate Supported is : 3.69M baud with < 0.1% Error rate

Parity : None, Even or Odd

Number of Stop Bits : 1 or 2

Bits per byte : 8



Note: The maximum baud rate is 2400 baud during deep sleep

5.2 I²C Interface

The I²C interface communicates to EEPROM, external peripherals or sensors. An EEPROM connection holds the program code inside the WC7220B0 module.

The EEPROM connected to the I²C interface where I2C_SCL, I2C_SDA and PIO[2] are connected to the external EEPROM. The PIO[2] pin supplies the power to the EEPROM supply pin, e.g. VDD. At boot up, if there is no valid ROM image in the WC7220B0 ROM area

it tries to boot from the I²C interface. This involves reading the code from the external EEPROM and loading it into the internal RAM.

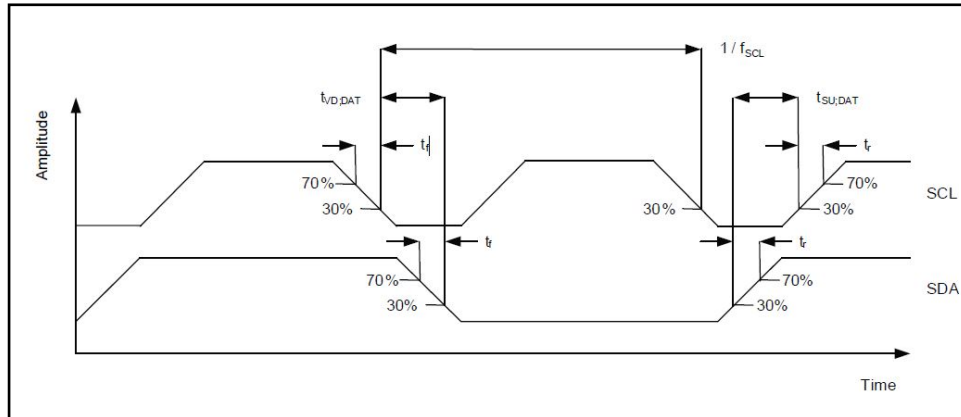


Figure 3: I²C standard mode 100 kHz timing diagram

Parameter	Symbol	Min	Max	Unit
Clock rate	f_{SCL}	-	100	kHz
SCL: Rise-time (30% to 70%)	t_r	-	50.3	ns
SCL: Fall-time (70% to 30%)	t_f	-	0.9	ns
SDA: Rise-time (30% to 70%)	t_r		55.3	ns
SDA: Fall-time (70% to 30%)	t_f		0.7	ns
Data set-up time	$t_{SU,DAT}$	2511	-	ns
Data valid time	$t_{VD,DAT}$	-	2.5	uS

Table 11: I²C standard mode 100 kHz timing definition

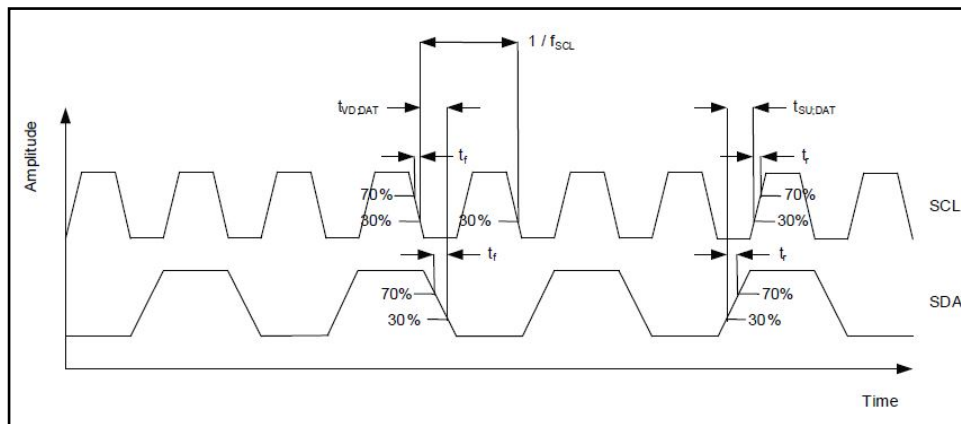


Figure 4: I²C fast mode 400 kHz timing diagram

Parameter	Symbol	Min	Max	Unit
Clock rate	f_{SCL}	-	400	kHz
SCL: Rise-time (30% to 70%)	t_r	41.4	50.6	ns
SCL: Fall-time (70% to 30%)	t_f	0.7	0.9	ns
SDA: Rise-time (30% to 70%)	t_r	46	55.9	ns
SDA: Fall-time (70% to 30%)	t_f	0.5	0.7	ns
Data set-up time	$t_{SU;DAT}$	573	-	ns
Data valid time	$t_{VD;DAT}$	-	0.56	uS

Table 12: I²C Fast Mode 400 kHz Timing Definition

6. Programming and Debug Interface

The WC7220B0 debug SPI interface is available in SPI slave mode to enable an external MCU to program and control the WC7220B0, generally via libraries or by tools supplied along with the package. The protocol of this interface is proprietary. The 4 SPI debug lines directly support this function. The SPI programs, configures and debugs the WC7220B0. It is required in production. Ensure the 4 SPI signals are brought out to either test points or a header. Take SPI_PIO# high to enable the SPI debug feature on PIO[8:5].

7. Reset

WC7220B0 is reset by:

- Power-on reset
- Software-configured watchdog timer

7.1 Digital Pin States on Reset

Table 14: Ordering Information for Modules shows the pin states of WC7220B0 on reset. PU and PD default to weak values unless specified otherwise.

Pin Name	Reset State
I2C_SDA	Strong Pull UP
I2C_SCL	Strong Pull UP
PIO[11:0]	Weak PD
AIO[2:0]	Weak PU

Table 13: Reset States of Pins

8. Antenna and Clock

- WC7220B0 has integrated chip antenna.
- WC7220B0 has 32.768 KHz and 16 MHz crystals internally.

9. Software Specifications

WC7220B0 is supplied with Bluetooth v4.1 specification compliant stack firmware. Figure 5: Software Architecture shows that the WC7220B0 software architecture enables the Bluetooth processing and the application program to run on the internal RISC MCU.

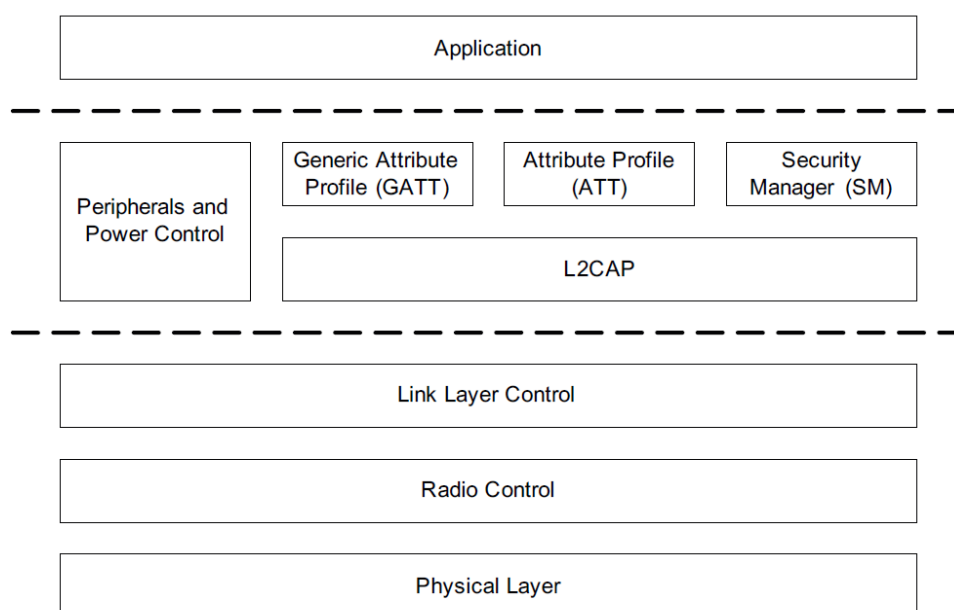
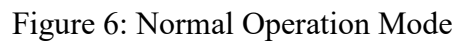


Figure 5: Software Architecture

The schematic in Figure 6: Normal Operation Mode shows the WC7220B0 connections.



11. Manufacturing Notes

11.1 Shield Marking

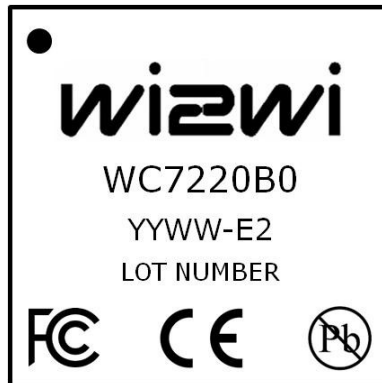


Figure 7: Shield Marking (Top View)

- YY indicates Year
- WW indicates Work Week
- E indicates Extended operating temperature range (-30°C to +85°C)
- 2 indicates Chip Antenna

11.2 Storage and Baking Instructions

WC7220B0 is an MSL3 qualified package. After opening the bag, the parts should be stored as per JSTD-033 standard, and Mounted within 168 hours of factory conditions ($\leq 30^{\circ}\text{C}$, 60% RH) If the parts have been exposed in transit, they need to be baked at 125°C for 16 hours.

11.3 Recommended Reflow Profile

Assembly Guidelines:

1. Follow solder paste manufacturers recommended profile
 - a. All RoHS solder pastes contain the same basic chemistry; however, each manufacturer may have a recommended reflow profile that performs best for their product.
2. The profile illustrated in JESD-020 and below is for reference only.
 - a. There is no one profile that fits all scenarios.
3. Profiles must be dialed in to the specific assembly type.
4. ENIG finishes are more susceptible to voids and air entrapment.
 - a. Selecting a RoHS solder paste that is “ENIG” compatible is recommended.
5. Recommended finishes for LGA/BGA inclusive assemblies include HASL, OSP, Tin, & Silver.

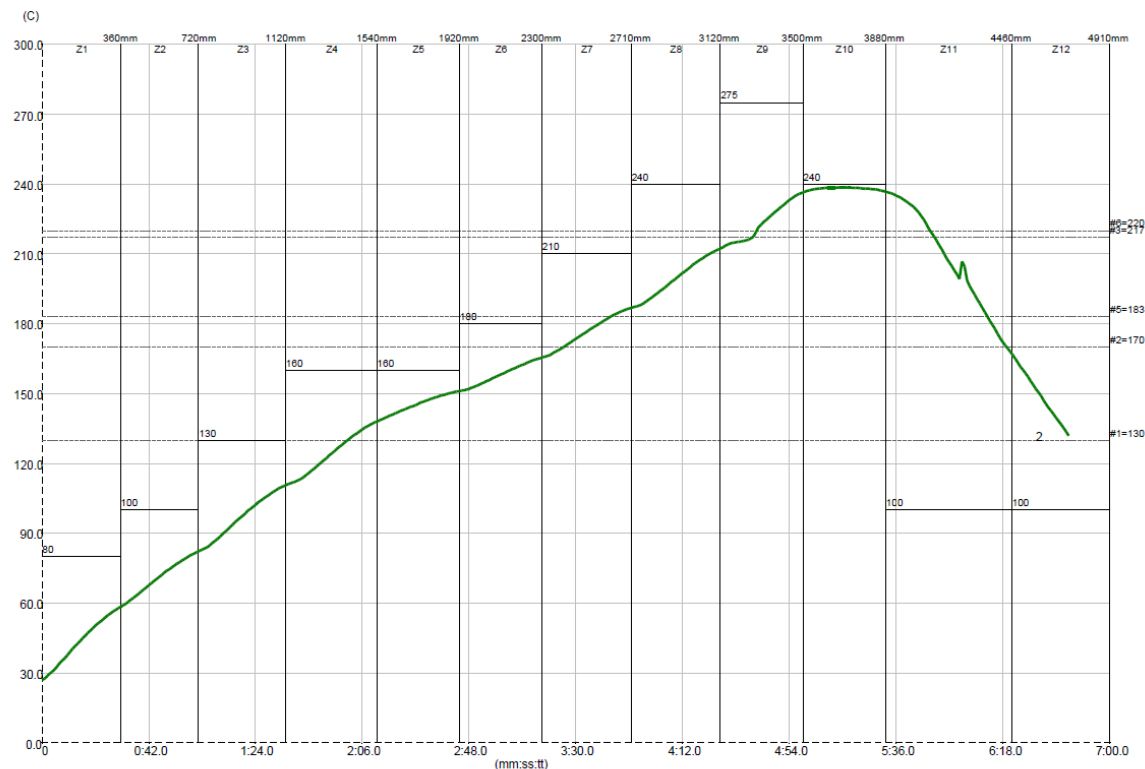


Figure 8: Recommended Reflow Profile

11.4 Data Sheet Status

Wi2Wi, Inc. reserves the right to change the specification without prior notice in order to improve the design and supply the best possible product. Updated information, firmware and release notes will be made available on www.wi2wi.com. Please check with Wi2Wi Inc. for the most recent data before initiating or completing a design.

12. Ordering Information

Part Order Number	Operating Temperature Range	Packaging Method
WC7220B0-E2QT	Extended: -30°C to +85°C	Tray
WC7220B0-E2QR	Extended: -30°C to +85°C	Tape & Reel

Table 14: Ordering Information for Modules

Part Order Number	Contents of the Evaluation Kit	Packaging Method
WC7220B0-DVK2	WC7220B0 Development Board, SPI Debugger, USB Mini and Micro cable, with all software and collaterals	Box

Table 15: Ordering Information for Development Kit

13. Certifications*

FCC, IC, CE

EMC/Immunity

Product Safety

*Certification under Progress

14. References

14.1 Specifications

Bluetooth Core Specification 4.1

14.2 Trademarks, Patents and Licenses

Trademarks: Bluetooth

14.3 Discloser

WC7220B0-DVK2: Development Kit

The specification maximum and minimum limits presented herein are those guaranteed when the unit is integrated into the Wi2Wi's WC7220B0-DVK2 Development System. These limits are to serve as representative performance characteristics of the WC7220B0 when properly designed into a customer's product. Wi2Wi makes no warranty, implied or otherwise specified, with respect to design and performance characteristics presented in this specification when used in customer designs.