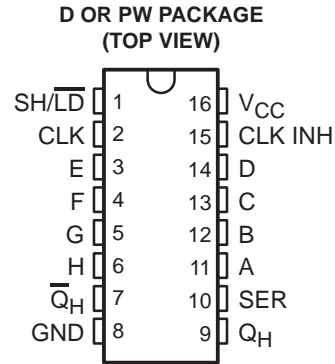


# SN74HC165-Q1 8-BIT PARALLEL-LOAD SHIFT REGISTER

SCLS518 – AUGUST 2003

- Qualification in Accordance With AEC-Q100†
- Qualified for Automotive Applications
- Customer-Specific Configuration Control Can Be Supported Along With Major-Change Approval
- ESD Protection Exceeds 1500 V Per MIL-STD-883, Method 3015; Exceeds 200 V Using Machine Model (C = 200 pF, R = 0)
- Wide Operating Voltage Range of 2 V to 6 V
- Outputs Can Drive Up To 10 LSTTL Loads
- Low Power Consumption, 80- $\mu$ A Max  $I_{CC}$
- Typical  $t_{pd} = 13$  ns
- $\pm 4$ -mA Output Drive at 5 V
- Low Input Current of 1  $\mu$ A Max
- Complementary Outputs
- Direct Overriding Load (Data) Inputs
- Gated Clock Inputs
- Parallel-to-Serial Data Conversion

† Contact factory for details. Q100 qualification data available on request.



## description/ordering information

The SN74HC165 is an 8-bit parallel-load shift register that, when clocked, shift the data toward a serial ( $Q_H$ ) output. Parallel-in access to each stage is provided by eight individual direct data (A–H) inputs that are enabled by a low level at the shift/load ( $SH/\overline{LD}$ ) input. The SN74HC165 also features a clock-inhibit (CLK INH) function and a complementary serial ( $\overline{Q}_H$ ) output.

Clocking is accomplished by a low-to-high transition of the clock (CLK) input while  $SH/\overline{LD}$  is held high and CLK INH is held low. The functions of CLK and CLK INH are interchangeable. Since a low CLK and a low-to-high transition of CLK INH also accomplish clocking, CLK INH should be changed to the high level only while CLK is high. Parallel loading is inhibited when  $SH/\overline{LD}$  is held high. While  $SH/\overline{LD}$  is low, the parallel inputs to the register are enabled independently of the levels of the CLK, CLK INH, or serial (SER) inputs.

## ORDERING INFORMATION

T <sub>A</sub>	PACKAGE‡		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 125°C	SOIC – D	Tape and reel	SN74HC165QDRQ1	HC165Q1
	TSSOP – PW	Tape and reel	SN74HC165QPWRQ1	HC165Q1

‡ Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

 **TEXAS  
INSTRUMENTS**

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# SN74HC165-Q1

## 8-BIT PARALLEL-LOAD SHIFT REGISTER

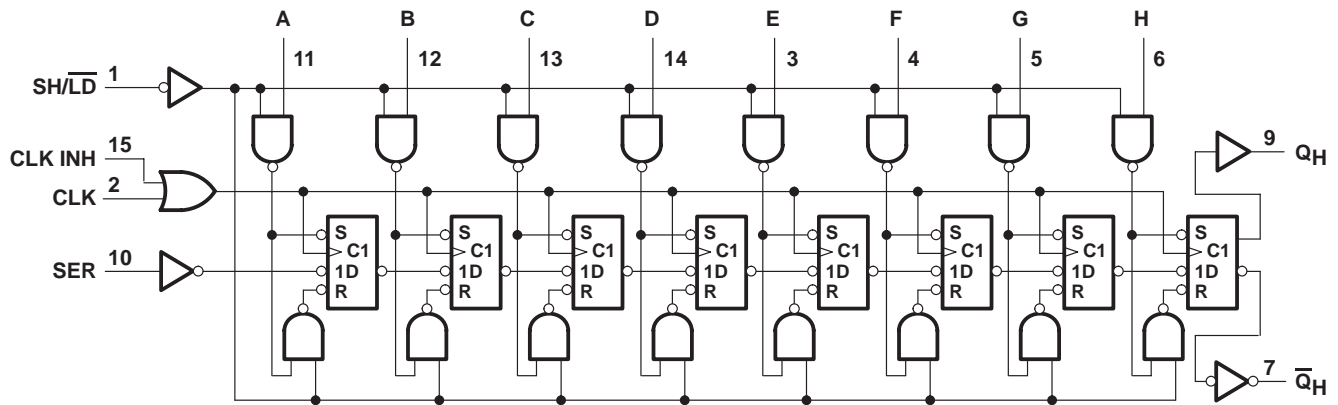
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FUNCTION TABLE

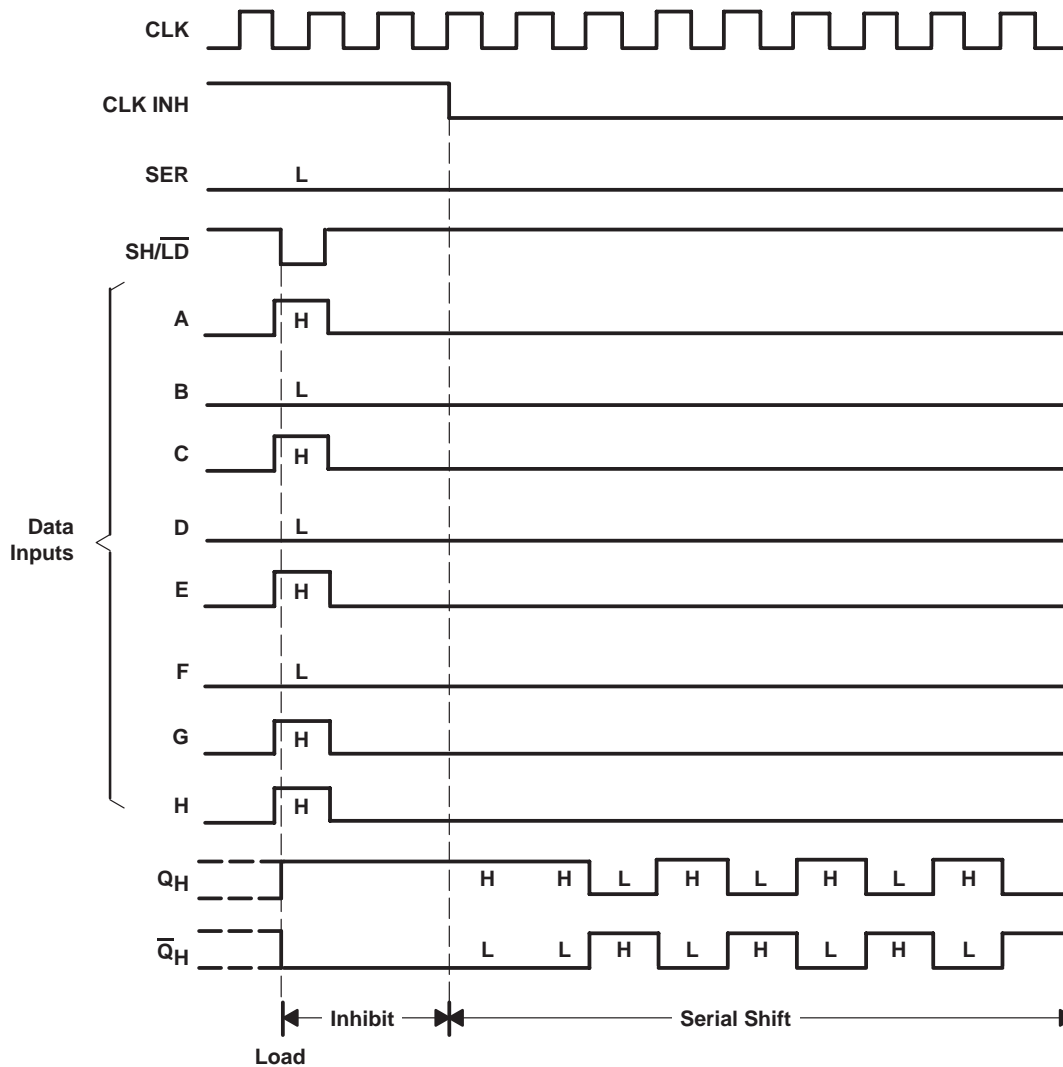
INPUTS			FUNCTION
SH/LD	CLK	CLK INH	
L	X	X	Parallel load
H	H	X	No change
H	X	H	No change
H	L	↑	Shift†
H	↑	L	Shift†

† Shift = content of each internal register shifts toward serial output Q<sub>H</sub>. Data at SER is shifted into the first register.

### logic diagram (positive logic)



typical shift, load, and inhibit sequence



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## 8-BIT PARALLEL-LOAD SHIFT REGISTER

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### absolute maximum ratings over operating free-air temperature range (unless otherwise noted)<sup>†</sup>

Supply voltage range, $V_{CC}$	-0.5 V to 7 V
Input clamp current, $I_{IK}$ ( $V_I < 0$ or $V_I > V_{CC}$ ) (see Note 1)	±20 mA
Output clamp current, $I_{OK}$ ( $V_O < 0$ or $V_O > V_{CC}$ ) (see Note 1)	±20 mA
Continuous output current, $I_O$ ( $V_O = 0$ to $V_{CC}$ )	±25 mA
Continuous current through $V_{CC}$ or GND	±50 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): D package	73°C/W
PW package	108°C/W
Storage temperature range, $T_{stg}$	-65°C to 150°C

<sup>†</sup> Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.  
 2. The package thermal impedance is calculated in accordance with JESD 51-7.

### recommended operating conditions (see Note 3)

		MIN	NOM	MAX	UNIT
$V_{CC}$	Supply voltage	2	5	6	V
$V_{IH}$	High-level input voltage	$V_{CC} = 2\text{ V}$	1.5		V
		$V_{CC} = 4.5\text{ V}$	3.15		
		$V_{CC} = 6\text{ V}$	4.2		
$V_{IL}$	Low-level input voltage	$V_{CC} = 2\text{ V}$		0.5	V
		$V_{CC} = 4.5\text{ V}$		1.35	
		$V_{CC} = 6\text{ V}$		1.8	
$V_I$	Input voltage	0		$V_{CC}$	V
$V_O$	Output voltage	0		$V_{CC}$	V
$\Delta t/\Delta v^\ddagger$	Input transition rise/fall time	$V_{CC} = 2\text{ V}$		1000	ns
		$V_{CC} = 4.5\text{ V}$		500	
		$V_{CC} = 6\text{ V}$		400	
$T_A$	Operating free-air temperature	-40		125	°C

NOTE 3: All unused inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

<sup>‡</sup> If this device is used in the threshold region (from  $V_{ILmax} = 0.5\text{ V}$  to  $V_{IHmin} = 1.5\text{ V}$ ), there is a potential to go into the wrong state from induced grounding, causing double clocking. Operating with the inputs at  $t_t = 1000\text{ ns}$  and  $V_{CC} = 2\text{ V}$  does not damage the device; however, functionally, the CLK inputs are not ensured while in the shift, count, or toggle operating modes.



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## 8-BIT PARALLEL-LOAD SHIFT REGISTER

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
			MIN	TYP	MAX			
V <sub>OH</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -20 μA	2 V	1.9	1.998	1.9		V
			4.5 V	4.4	4.499	4.4		
			6 V	5.9	5.999	5.9		
		I <sub>OH</sub> = -4 mA	4.5 V	3.98	4.3	3.7		
			6 V	5.48	5.8	5.2		
V <sub>OL</sub>	V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 20 μA	2 V	0.002 0.1		0.1		V
			4.5 V	0.001 0.1		0.1		
			6 V	0.001 0.1		0.1		
		I <sub>OL</sub> = 4 mA	4.5 V	0.17 0.26		0.4		
			6 V	0.15 0.26		0.4		
I <sub>I</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0	6 V	±0.1 ±100		±1000		nA	
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or 0, I <sub>O</sub> = 0	6 V			8 160		μA	
C <sub>i</sub>		2 V to 6 V	3 10		10		pF	

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## 8-BIT PARALLEL-LOAD SHIFT REGISTER

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timing requirements over recommended operating free-air temperature range (unless otherwise noted)

		V <sub>CC</sub>	T <sub>A</sub> = 25°C		MIN	MAX	UNIT
			MIN	MAX			
f <sub>clock</sub>	Clock frequency	2 V	6		4.2		MHz
		4.5 V	31		21		
		6 V	36		25		
t <sub>w</sub>	SH/ $\overline{\text{LD}}$ low	2 V	80		120		ns
		4.5 V	16		24		
		6 V	14		20		
	CLK high or low	2 V	80		120		
		4.5 V	16		24		
		6 V	14		20		
t <sub>su</sub>	SH/ $\overline{\text{LD}}$ high before CLK $\uparrow$	2 V	80		120		ns
		4.5 V	16		24		
		6 V	14		20		
	SER before CLK $\uparrow$	2 V	40		60		
		4.5 V	8		12		
		6 V	7		10		
	CLK INH low before CLK $\uparrow$	2 V	100		150		
		4.5 V	20		30		
		6 V	17		25		
	CLK INH high before CLK $\uparrow$	2 V	40		60		
		4.5 V	8		12		
		6 V	7		10		
	Data before SH/ $\overline{\text{LD}}$ $\downarrow$	2 V	100		150		
		4.5 V	20		30		
		6 V	17		26		
t <sub>h</sub>	SER data after CLK $\uparrow$	2 V	5		5		ns
		4.5 V	5		5		
		6 V	5		5		
	PAR data after SH/ $\overline{\text{LD}}$ $\downarrow$	2 V	5		5		
		4.5 V	5		5		
		6 V	5		5		

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## 8-BIT PARALLEL-LOAD SHIFT REGISTER

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switching characteristics over recommended operating free-air temperature range,  $C_L = 50 \text{ pF}$  (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V <sub>CC</sub>	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
f <sub>max</sub>			2 V	6	13		4.2	MHz	
			4.5 V	31	50		21		
			6 V	36	62		25		
t <sub>pd</sub>	SH/ $\overline{\text{LD}}$	Q <sub>H</sub> or $\overline{\text{Q}}_H$	2 V		80	150		225	ns
			4.5 V		20	30		45	
			6 V		16	26		38	
	CLK	Q <sub>H</sub> or $\overline{\text{Q}}_H$	2 V		75	150		225	
			4.5 V		15	30		45	
			6 V		13	26		38	
	H	Q <sub>H</sub> or $\overline{\text{Q}}_H$	2 V		75	150		225	
			4.5 V		15	30		45	
			6 V		13	26		38	
t <sub>t</sub>		Any	2 V		38	75		110	ns
			4.5 V		8	15		22	
			6 V		6	13		19	

operating characteristics, T<sub>A</sub> = 25°C

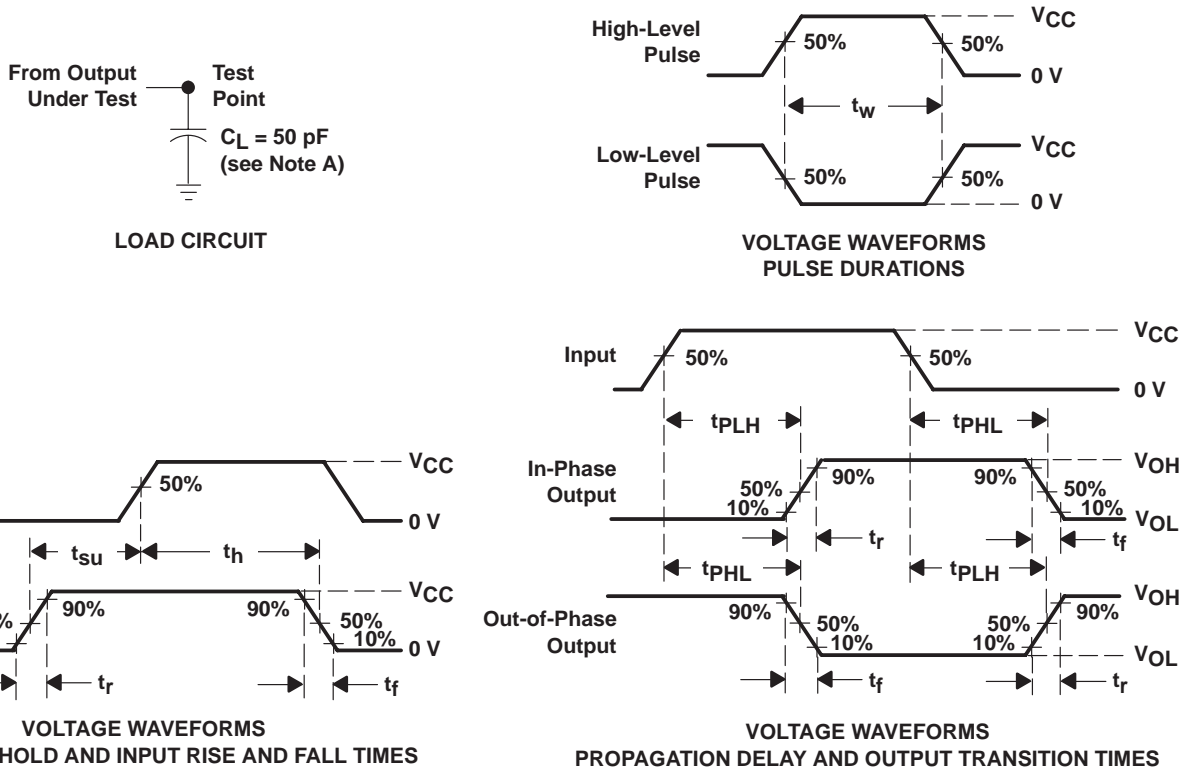
PARAMETER	TEST CONDITIONS	TYP	UNIT
C <sub>pd</sub> Power dissipation capacitance	No load	75	pF

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## 8-BIT PARALLEL-LOAD SHIFT REGISTER

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### PARAMETER MEASUREMENT INFORMATION



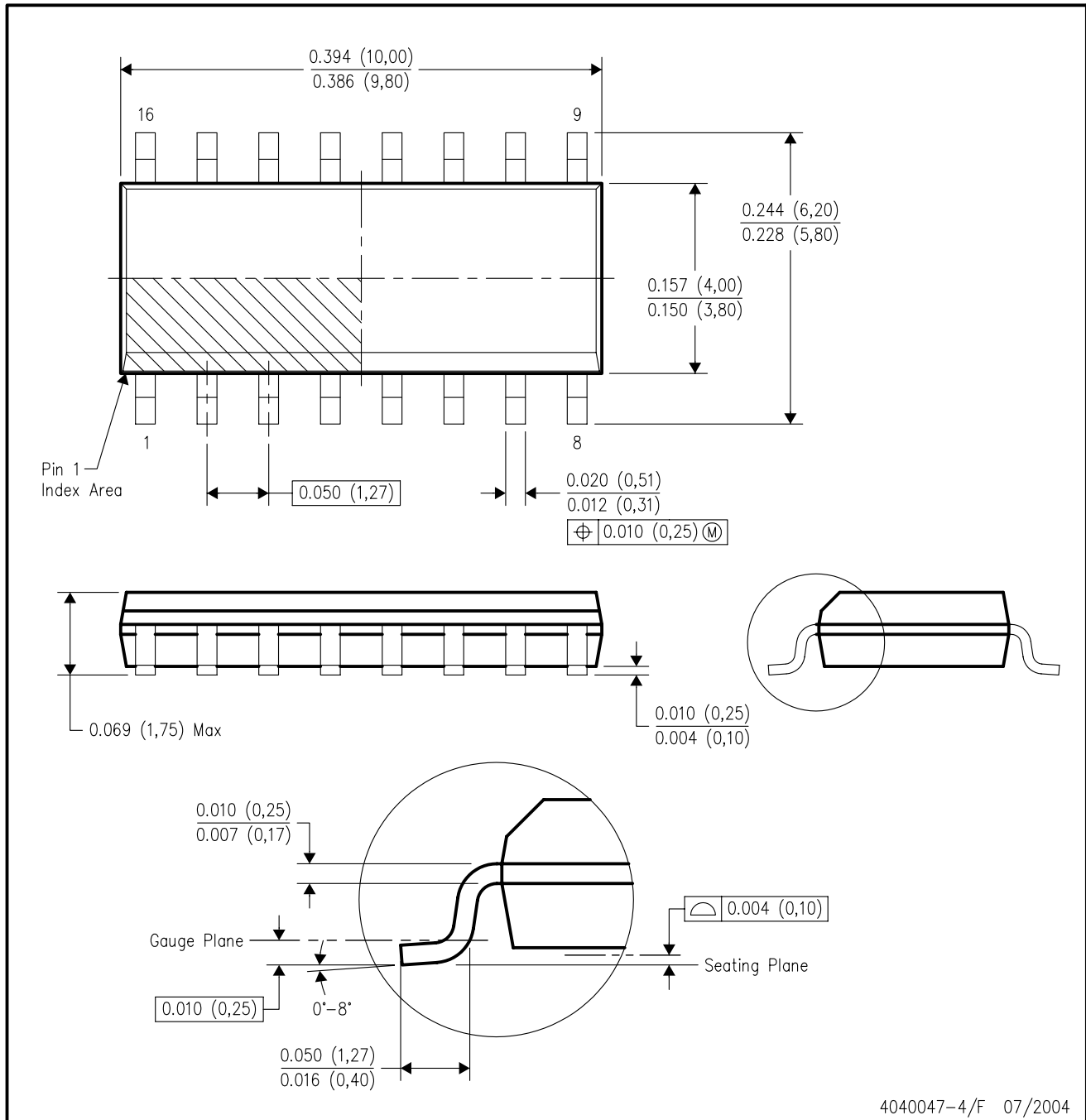
- NOTES:
- A.  $C_L$  includes probe and test-fixture capacitance.
  - B. Phase relationships between waveforms were chosen arbitrarily. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r = 6 \text{ ns}$ ,  $t_f = 6 \text{ ns}$ .
  - C. For clock inputs,  $f_{max}$  is measured when the input duty cycle is 50%.
  - D. The outputs are measured one at a time with one input transition per measurement.
  - E.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .

Figure 1. Load Circuit and Voltage Waveforms



D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
  - D. Falls within JEDEC MS-012 variation AC.

PW (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14 PINS SHOWN



4040064/F 01/97

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-153

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