

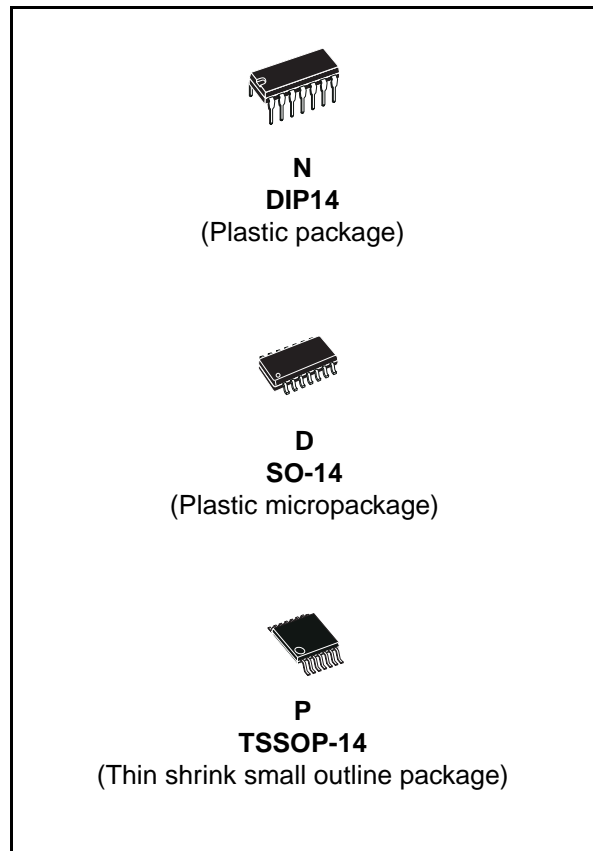
## Low power quad operational amplifiers

### Features

- Wide gain bandwidth: 1.3 MHz
- Input common-mode voltage range includes ground
- Large voltage gain: 100 dB
- Very low supply current per amplifier: 375  $\mu$ A
- Low input bias current: 20 nA
- Low input offset voltage: 5 mV max. (For more accurate applications, use the equivalent parts LM124A-LM224A-LM324A which feature 3 mV max.)
- Low input offset current: 2 nA
- Wide power supply range:
  - Single supply: +3 V to +30 V
  - Dual supplies:  $\pm$ 1.5 V to  $\pm$ 15 V

### Description

These circuits consist of four independent, high gain, internally frequency compensated operational amplifiers. They operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.



### Order codes

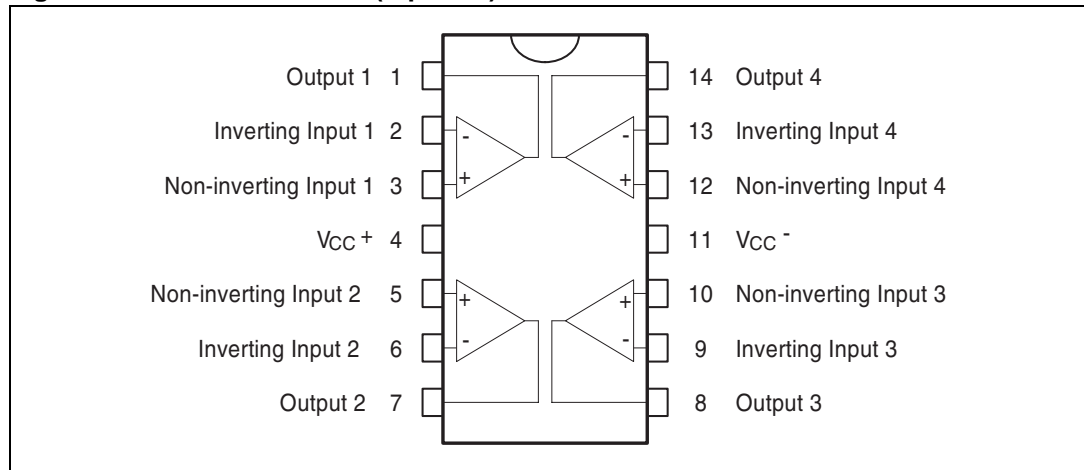
Part number	Temperature range	Package	Packing
LM124N	-55°C, +125°C	DIP	Tube
LM124D/DT		SO	Tube or tape & reel
LM224N	-40°C, +105°C	DIP	Tube
LM224D/DT		SO	Tube or tape & reel
LM224PT		TSSOP (Thin shrink outline package)	Tape & reel
LM324N	0°C, +70°C	DIP	Tube
LM324D/DT		SO	Tube or tape & reel
LM324PT		TSSOP (Thin shrink outline package)	Tape & reel

# Contents

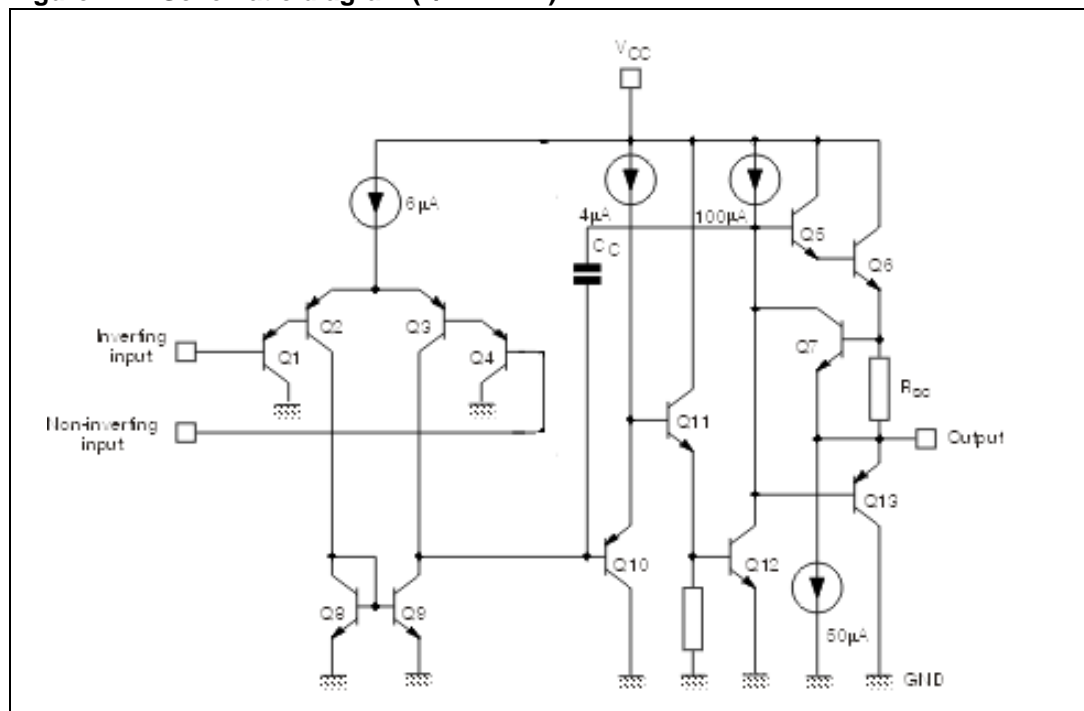
<b>1</b>	<b>Pin &amp; schematic diagram</b> .....	<b>3</b>
<b>2</b>	<b>Absolute maximum ratings</b> .....	<b>4</b>
<b>3</b>	<b>Electrical characteristics</b> .....	<b>5</b>
<b>4</b>	<b>Typical single-supply applications</b> .....	<b>10</b>
<b>5</b>	<b>Macromodels</b> .....	<b>12</b>
<b>6</b>	<b>Package information</b> .....	<b>14</b>
6.1	DIP14 package .....	15
6.2	SO-14 package .....	16
6.3	TSSOP14 package .....	17
<b>7</b>	<b>Revision history</b> .....	<b>18</b>

# 1 Pin & schematic diagram

**Figure 1. Pin connections (top view)**



**Figure 2. Schematic diagram (1/4 LM124)**



## 2 Absolute maximum ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	LM124	LM224	LM324	Unit
$V_{CC}$	Supply voltage	±16 or 32			V
$V_i$	Input voltage	32			V
$V_{id}$	Differential input voltage <sup>(1)</sup>	32			V
$P_{tot}$	Power dissipation	500	500	500	mW
	N suffix				
	Output short-circuit duration <sup>(2)</sup>	Infinite			
$I_{in}$	Input current <sup>(3)</sup>	50	50	50	mA
$T_{oper}$	Operating free-air temperature range	-55 to +125	-40 to +105	0 to +70	°C
$T_{stg}$	Storage temperature range	-65 to +150			°C
$T_j$	Maximum junction temperature	150			°C
$R_{thja}$	Thermal resistance junction to ambient <sup>(4)</sup>				°C/W
	SO14	103			
	TSSOP14	100			
$R_{thjc}$	Thermal resistance junction to case				°C/W
	SO14	31			
	TSSOP14	32			
ESD	HBM: human body model <sup>(5)</sup>	250			V
	MM: machine model <sup>(6)</sup>	150			
	CDM: charged device model	1500			

1. Either or both input voltages must not exceed the magnitude of  $V_{CC}^+$  or  $V_{CC}^-$ .
2. Short-circuits from the output to  $V_{CC}$  can cause excessive heating if  $V_{CC} > 15V$ . The maximum output current is approximately 40 mA independent of the magnitude of  $V_{CC}$ . Destructive dissipation can result from simultaneous short-circuits on all amplifiers.
3. This input current only exists when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistor becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also NPN parasitic action on the IC chip. This transistor action can cause the output voltages of the op-amps to go to the  $V_{CC}$  voltage level (or to ground for a large overdrive) for the time during which an input is driven negative. This is not destructive and normal output is restored for input voltages above -0.3 V.
4. Short-circuits can cause excessive heating. Destructive dissipation can result from simultaneous short-circuits on all amplifiers. These are typical values given for a single layer board (except for TSSOP, a two-layer board).
5. Human body model, 100 pF discharged through a 1.5 kΩ resistor into pin of device.
6. Machine model ESD, a 200 pF cap is charged to the specified voltage, then discharged directly into the IC with no external series resistor (internal resistor < 5 Ω), into pin-to-pin of device.

### 3 Electrical characteristics

Table 2.  $V_{CC}^+ = +5\text{ V}$ ,  $V_{CC}^- = \text{Ground}$ ,  $V_o = 1.4\text{ V}$ ,  $T_{\text{amb}} = +25^\circ\text{ C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$V_{io}$	Input offset voltage <sup>(1)</sup> $T_{\text{amb}} = +25^\circ\text{ C}$ LM124-LM224 LM324		2	5 7	mV
	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ LM124-LM224 LM324			7 9	
$I_{io}$	Input offset current $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$		2	30 100	nA
$I_{ib}$	Input bias current <sup>(2)</sup> $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$		20	150 300	nA
$A_{vd}$	Large signal voltage gain $V_{CC}^+ = +15\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $V_o = 1.4\text{ V to } 11.4\text{ V}$ $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	50 25	100		V/mV
SVR	Supply voltage rejection ratio ( $R_s \leq 10\text{ k}\Omega$ ) $V_{CC}^+ = 5\text{ V to } 30\text{ V}$ $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	65 65	110		dB
$I_{CC}$	Supply current, all Amp, no load $T_{\text{amb}} = +25^\circ\text{ C}$ $V_{CC} = +5\text{ V}$ $V_{CC} = +30\text{ V}$		0.7 1.5	1.2 3	mA
	$T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$ $V_{CC} = +5\text{ V}$ $V_{CC} = +30\text{ V}$		0.8 1.5	1.2 3	
$V_{icm}$	Input common mode voltage range $V_{CC} = +30\text{ V}$ <sup>(3)</sup> $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	0 0		$V_{CC} - 1.5$ $V_{CC} - 2$	V
CMR	Common mode rejection ratio ( $R_s \leq 10\text{ k}\Omega$ ) $T_{\text{amb}} = +25^\circ\text{ C}$ $T_{\text{min}} \leq T_{\text{amb}} \leq T_{\text{max}}$	70 60	80		dB
$I_{\text{source}}$	Output current source ( $V_{id} = +1\text{ V}$ ) $V_{CC} = +15\text{ V}$ , $V_o = +2\text{ V}$	20	40	70	mA

**Table 2.**  $V_{CC}^+ = +5\text{ V}$ ,  $V_{CC}^- = \text{Ground}$ ,  $V_o = 1.4\text{ V}$ ,  $T_{amb} = +25^\circ\text{ C}$  (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit
$I_{sink}$	Output sink current ( $V_{id} = -1\text{ V}$ )				
	$V_{CC} = +15\text{ V}$ , $V_o = +2\text{ V}$ $V_{CC} = +15\text{ V}$ , $V_o = +0.2\text{ V}$	10 12	20 50		mA $\mu\text{A}$
$V_{OH}$	High level output voltage $V_{CC} = +30\text{ V}$ $T_{amb} = +25^\circ\text{ C}$ , $R_L = 2\text{ k}\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$ $T_{amb} = +25^\circ\text{ C}$ , $R_L = 10\text{ k}\Omega$ $T_{min} \leq T_{amb} \leq T_{max}$	26 26 27 27	27 28		V
	$V_{CC} = +5\text{ V}$ , $R_L = 2\text{ k}\Omega$ $T_{amb} = +25^\circ\text{ C}$ $T_{min} \leq T_{amb} \leq T_{max}$	3.5 3			
$V_{OL}$	Low level output voltage ( $R_L = 10\text{ k}\Omega$ ) $T_{amb} = +25^\circ\text{ C}$ $T_{min} \leq T_{amb} \leq T_{max}$		5	20 20	mV
SR	Slew rate $V_{CC} = 15\text{ V}$ , $V_i = 0.5\text{ to }3\text{ V}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$ , unity gain		0.4		V/ $\mu\text{s}$
GBP	Gain bandwidth product $V_{CC} = 30\text{ V}$ , $f = 100\text{ kHz}$ , $V_{in} = 10\text{ mV}$ , $R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$		1.3		MHz
THD	Total harmonic distortion $f = 1\text{ kHz}$ , $A_v = 20\text{ dB}$ , $R_L = 2\text{ k}\Omega$ , $V_o = 2\text{ V}_{pp}$ , $C_L = 100\text{ pF}$ , $V_{CC} = 30\text{ V}$		0.015		%
$e_n$	Equivalent input noise voltage $f = 1\text{ kHz}$ , $R_s = 100\ \Omega$ , $V_{CC} = 30\text{ V}$		40		$\frac{\text{nV}}{\sqrt{\text{Hz}}}$
$DV_{io}$	Input offset voltage drift		7	30	$\mu\text{V}/^\circ\text{C}$
$DI_{io}$	Input offset current drift		10	200	$\text{pA}/^\circ\text{C}$
$V_{o1}/V_{o2}$	Channel separation <sup>(4)</sup> $1\text{ kHz} \leq f \leq 20\text{ kHz}$		120		dB

- $V_o = 1.4\text{ V}$ ,  $R_s = 0\ \Omega$ ,  $5\text{ V} < V_{CC}^+ < 30\text{ V}$ ,  $0 < V_{ic} < V_{CC}^+ - 1.5\text{ V}$
- The direction of the input current is out of the IC. This current is essentially constant, independent of the state of the output so there is no change in the load on the input lines.
- The input common-mode voltage of either input signal voltage should not be allowed to go negative by more than 0. V. The upper end of the common-mode voltage range is  $V_{CC}^+ - 1.5\text{ V}$ , but either or both inputs can go to +32 V without damage.
- Due to the proximity of external components, ensure that stray capacitance between these external parts does not cause coupling. Typically, this can be detected because this type of capacitance increases at higher frequencies.

Figure 3. Input bias current vs. ambient temperature

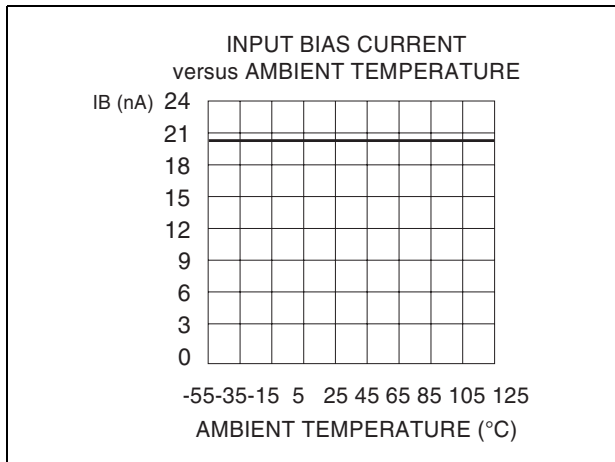


Figure 4. Current limiting

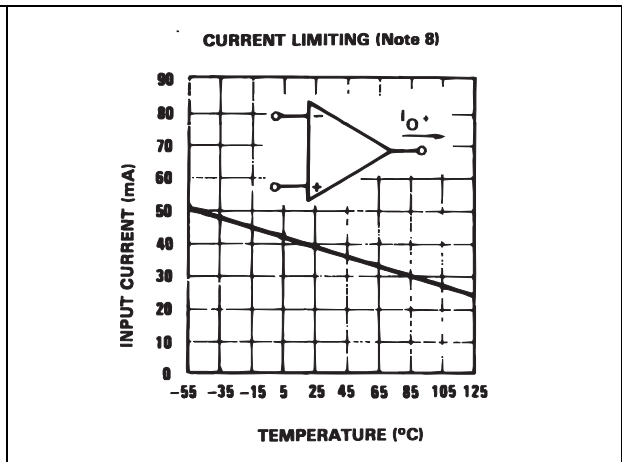


Figure 5. Input voltage range

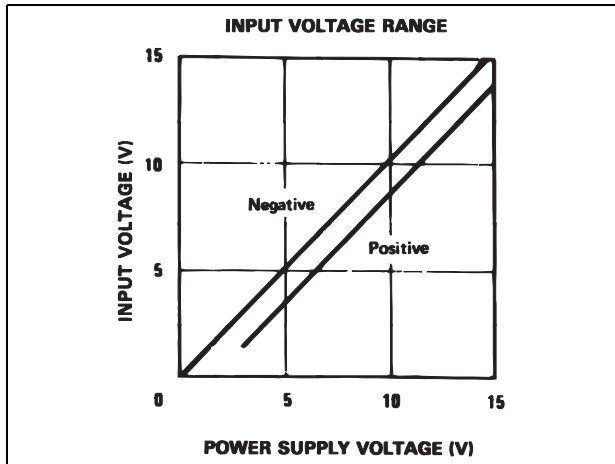


Figure 6. Supply current

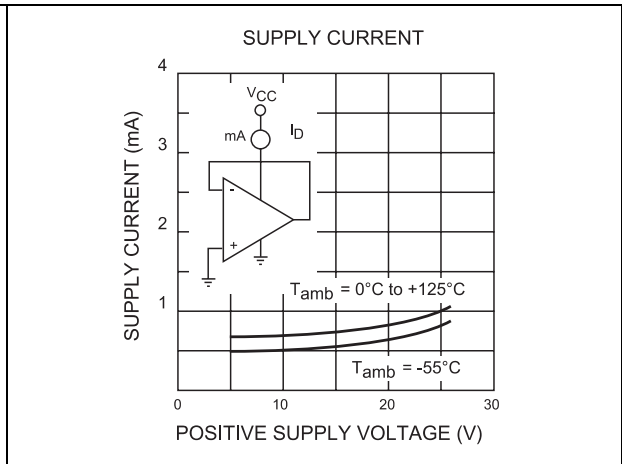


Figure 7. Gain bandwidth product

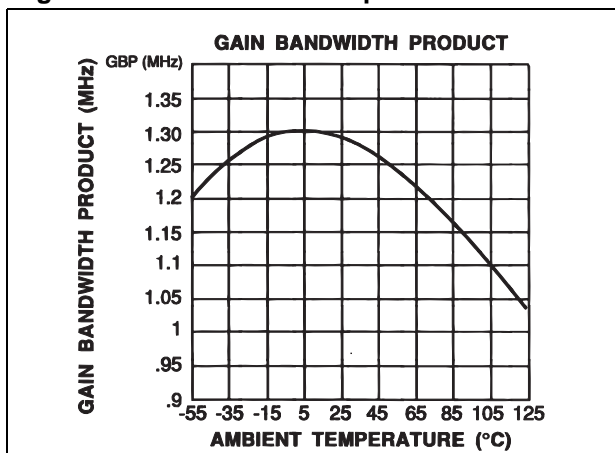
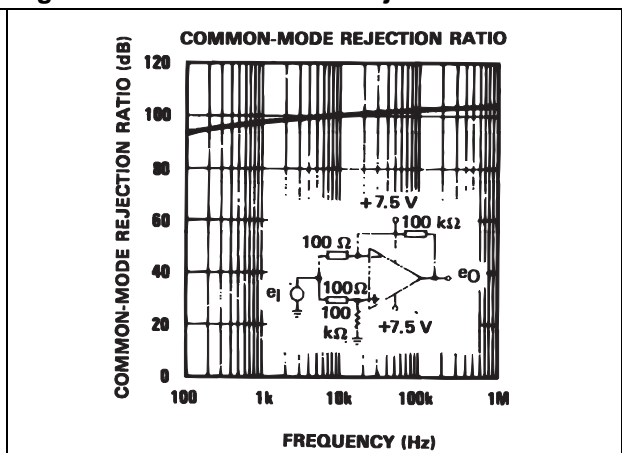


Figure 8. Common mode rejection ratio



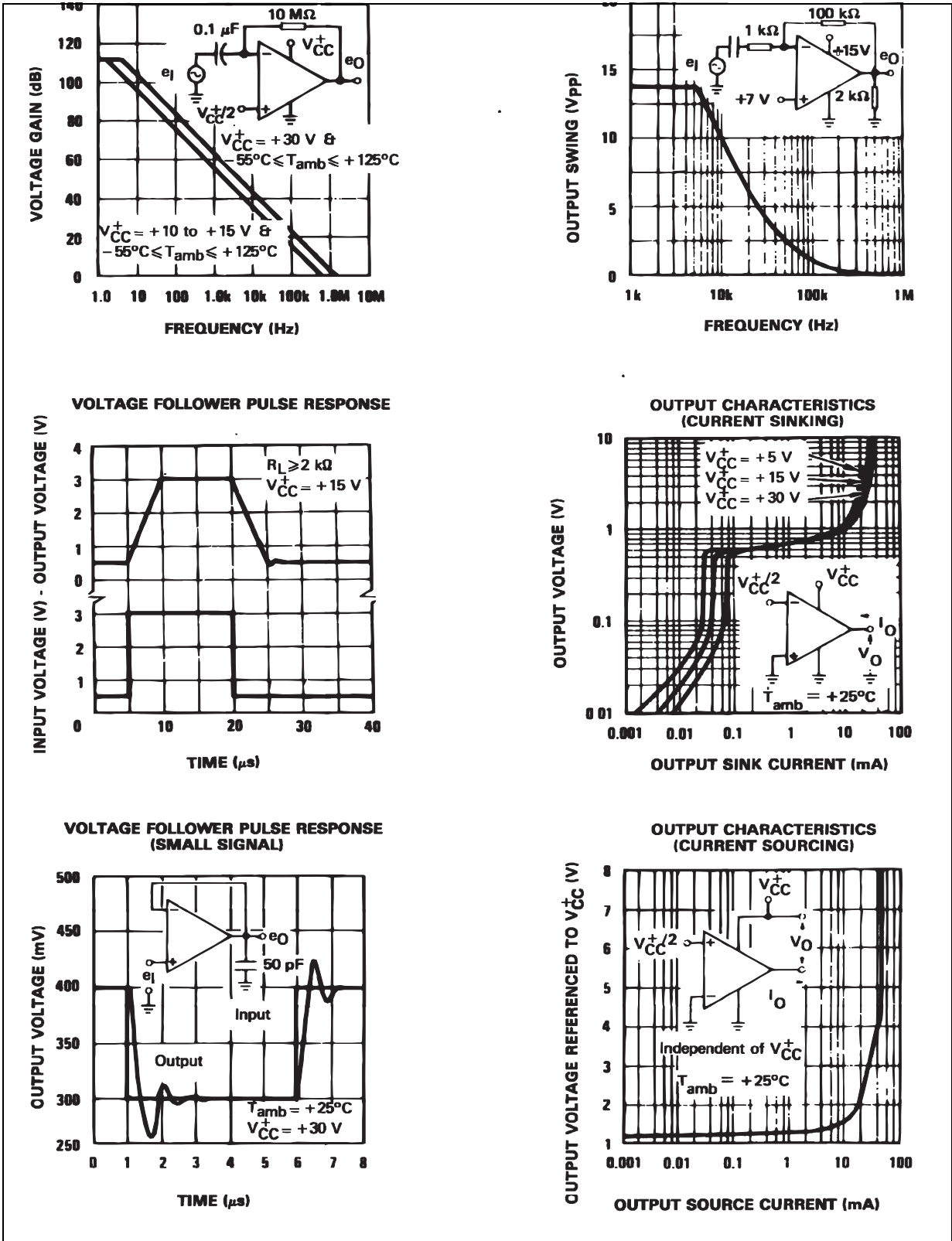




Figure 9. Input current

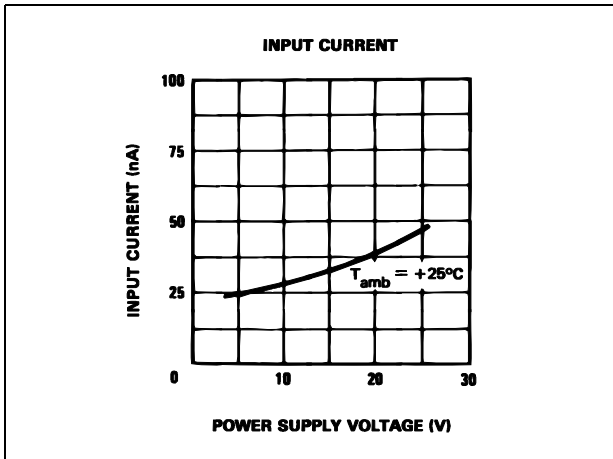


Figure 10. Large signal voltage gain

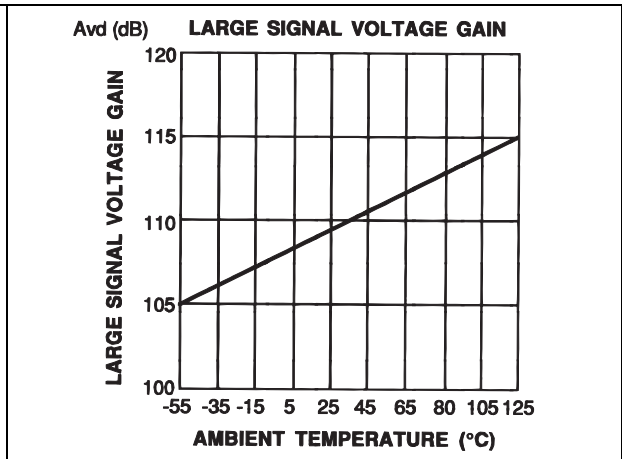


Figure 11. Power supply & common mode rejection ratio

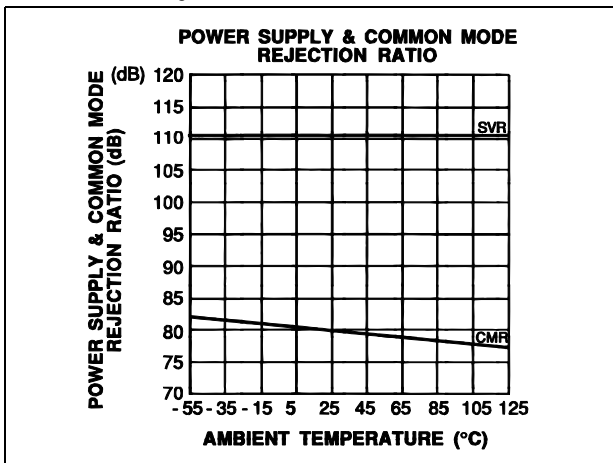
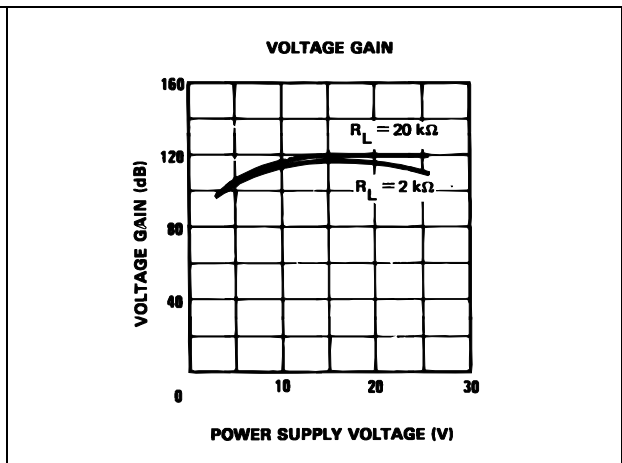


Figure 12. Voltage gain



# 4 Typical single-supply applications

Figure 13. AC coupled inverting amplifier

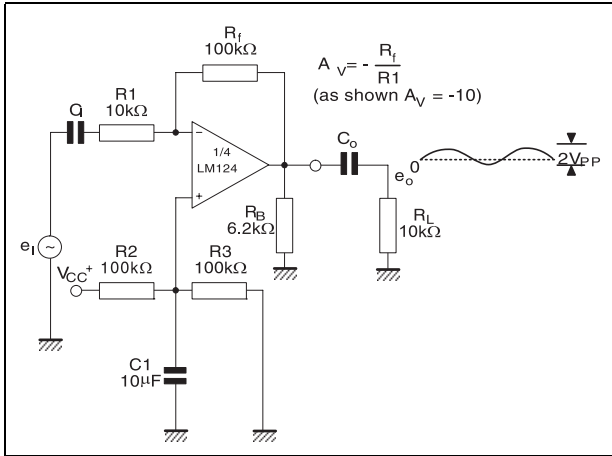


Figure 14. High input Z adjustable gain DC instrumentation amplifier

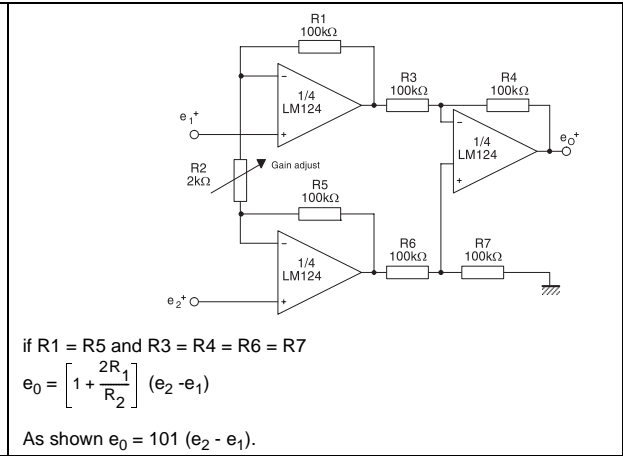


Figure 15. AC coupled non inverting amplifier

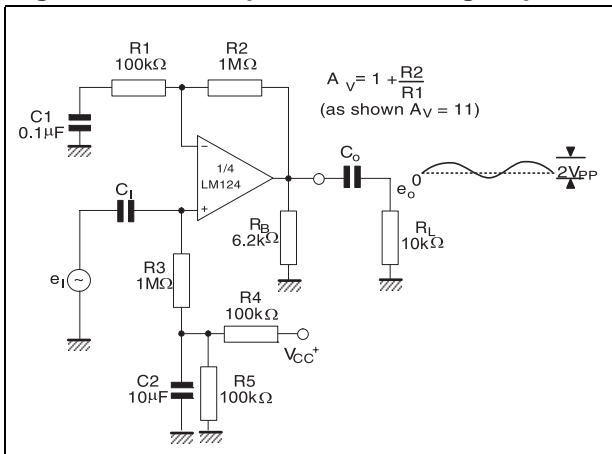


Figure 16. DC summing amplifier

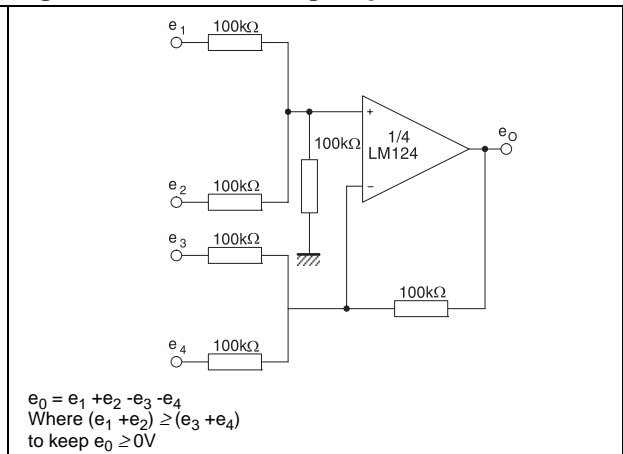


Figure 17. Non-inverting DC gain

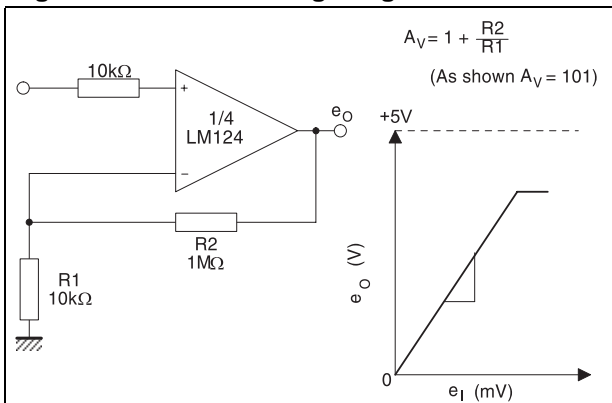


Figure 18. Low drift peak detector

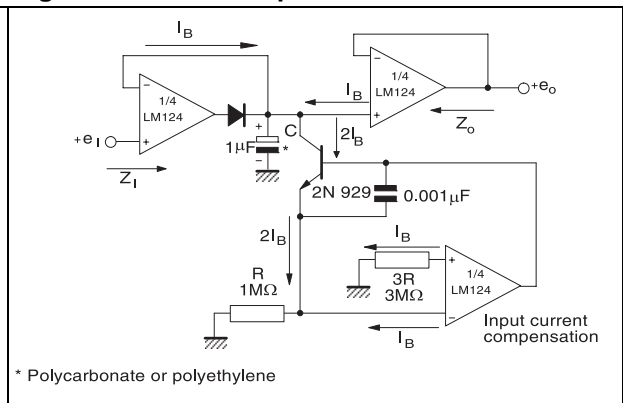


Figure 19. Active bandpass filter

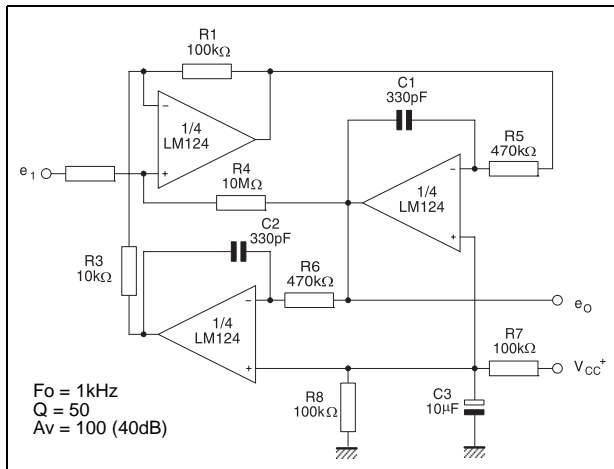


Figure 20. High input Z, DC differential amplifier

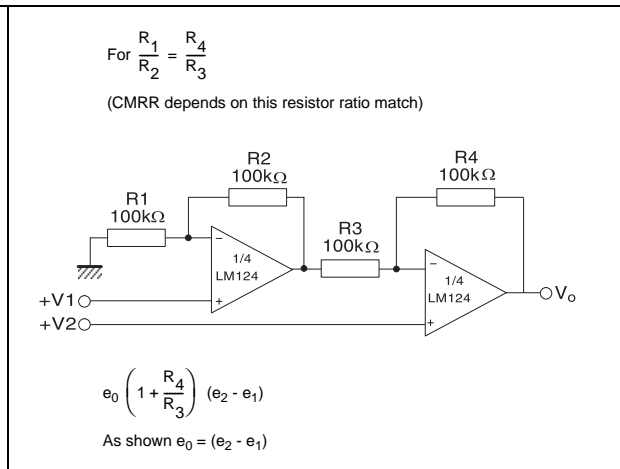
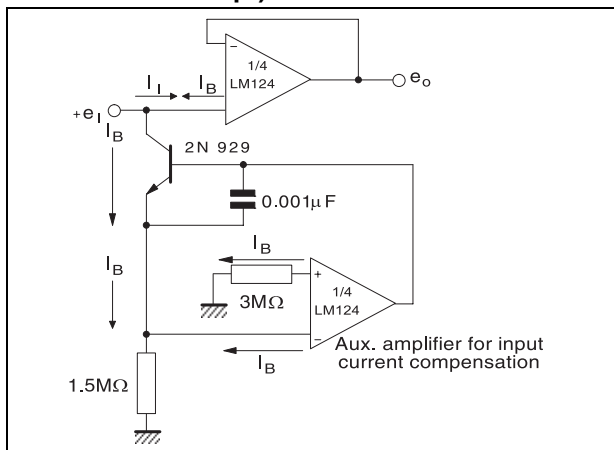


Figure 21. Using symmetrical amplifiers to reduce input current (general concept)



## 5 Macromodels

*Note: Please consider the following before using this macromodel:*

*All models are a trade-off between accuracy and complexity (i.e. simulation time).*

*Macromodels are not a substitute to breadboarding; rather, they confirm the validity of a design approach and help to select surrounding component values.*

*A macromodel emulates the **nominal** performance of a **typical** device within **specified operating conditions** (temperature, supply voltage, etc.). Thus the macromodel is often not as exhaustive as the datasheet, its purpose is to illustrate the main parameters of the product.*

*Data derived from macromodels that is used outside of the specified conditions ( $V_{CC}$ , temperature, etc.) or even worse, outside of the device operating conditions ( $V_{CC}$ ,  $V_{icm}$ , etc.) is not reliable in any way.*

```
** Standard Linear Ics Macromodels, 1993.
** CONNECTIONS :
* 1 INVERTING INPUT
* 2 NON-INVERTING INPUT
* 3 OUTPUT
* 4 POSITIVE POWER SUPPLY
* 5 NEGATIVE POWER SUPPLY

.SUBCKT LM124 1 3 2 4 5
*****
.MODEL MDTH D IS=1E-8 KF=3.104131E-15 CJO=10F
* INPUT STAGE
CIP 2 5 1.000000E-12
CIN 1 5 1.000000E-12
EIP 10 5 2 5 1
EIN 16 5 1 5 1
RIP 10 11 2.600000E+01
RIN 15 16 2.600000E+01
RIS 11 15 2.003862E+02
DIP 11 12 MDTH 400E-12
DIN 15 14 MDTH 400E-12
VOFP 12 13 DC 0
VOFN 13 14 DC 0
IPOL 13 5 1.000000E-05
CPS 11 15 3.783376E-09
DINN 17 13 MDTH 400E-12
VIN 17 5 0.000000E+00
DINR 15 18 MDTH 400E-12
VIP 4 18 2.000000E+00
FCP 4 5 VOFP 3.400000E+01
FCN 5 4 VOFN 3.400000E+01
FIBP 2 5 VOFN 2.000000E-03
FIBN 5 1 VOFP 2.000000E-03
* AMPLIFYING STAGE
FIP 5 19 VOFP 3.600000E+02
FIN 5 19 VOFN 3.600000E+02
```

```

RG1 19 5 3.652997E+06
RG2 19 4 3.652997E+06
CC 19 5 6.000000E-09
DOPM 19 22 MDTH 400E-12
DONM 21 19 MDTH 400E-12
HOPM 22 28 VOUT 7.500000E+03
VIPM 28 4 1.500000E+02
HONM 21 27 VOUT 7.500000E+03
VINM 5 27 1.500000E+02
EOUT 26 23 19 5 1
VOUT 23 5 0
ROUT 26 3 20
COUT 3 5 1.000000E-12
DOP 19 25 MDTH 400E-12
VOP 4 25 2.242230E+00
DON 24 19 MDTH 400E-12
VON 24 5 7.922301E-01
.ENDS

```

The values provided in [Table 3](#) are derived from this macromodel.

**Table 3.**  $V_{CC}^+ = +15V$ ,  $V_{CC}^- = 0V$ ,  $T_{amb} = 25^\circ C$  (unless otherwise specified)

Symbol	Conditions	Value	Unit
$V_{io}$		0	mV
$A_{vd}$	$R_L = 2\text{ k}\Omega$	100	V/mV
$I_{cc}$	No load, per amplifier	350	$\mu A$
$V_{icm}$		-15 to +13.5	V
$V_{OH}$	$R_L = 2\text{ k}\Omega$ ( $V_{CC}^+ = 15V$ )	+13.5	V
$V_{OL}$	$R_L = 10\text{ k}\Omega$	5	mV
$I_{os}$	$V_o = +2\text{ V}$ , $V_{CC} = +15\text{ V}$	+40	mA
GBP	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	1.3	MHz
SR	$R_L = 2\text{ k}\Omega$ , $C_L = 100\text{ pF}$	0.4	V/ $\mu s$

## 6 Package information

In order to meet environmental requirements, STMicroelectronics offers these devices in ECOPACK<sup>®</sup> packages. These packages have a Lead-free second level interconnect. The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an STMicroelectronics trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com).

## 6.1 DIP14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
a1	0.51			0.020		
B	1.39		1.65	0.055		0.065
b		0.5			0.020	
b1		0.25			0.010	
D			20			0.787
E		8.5			0.335	
e		2.54			0.100	
e3		15.24			0.600	
F			7.1			0.280
l			5.1			0.201
L		3.3			0.130	
Z	1.27		2.54	0.050		0.100

The figure contains three mechanical drawings of the DIP14 package. The top drawing is a perspective view showing the package body and the leads. Dimensions labeled include:  $a_1$  (lead thickness),  $B$  (lead width),  $b$  (lead thickness at the base),  $b_1$  (lead thickness at the top),  $e$  (lead pitch),  $e_3$  (total lead length),  $F$  (package height),  $l$  (lead length), and  $Z$  (lead diameter). The middle drawing is a side view showing the package body and the leads. Dimensions labeled include:  $E$  (package width) and  $b_1$  (lead thickness at the top). The bottom drawing is a top view of the package showing the pin layout. Dimensions labeled include:  $D$  (package length) and  $F$  (package height). Pin numbers 1, 7, 8, and 14 are indicated on the package body.

## 6.2 SO-14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.75			0.068
A1	0.1		0.2	0.003		0.007
A2			1.65			0.064
B	0.35		0.46	0.013		0.018
c	0.19		0.25	0.007		0.010
c1	45° (typ.)					
D	8.55		8.75	0.336		0.344
H	5.8		6.2	0.228		0.244
e		1.27			0.050	
E	3.8		4.0	0.149		0.157
L	0.5		0.127	0.019		0.050
k	8° (max.)					

The technical drawings illustrate the SO-14 package geometry. The side view shows dimensions A, A1, A2, B, and D. The top view shows dimensions E, H, L, and e. The detail view shows the lead profile with dimensions c, c1, and k. A note 'ddd C' is present in the side view, and 'SEATING PLANE C' and '0,25 mm GAGE PLANE' are indicated in the detail view.



### 6.3 TSSOP14 package

Ref.	Dimensions					
	Millimeters			Inches		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			1.2			0.047
A1	0.05	0.010	0.15	0.002	0.004	0.006
A2	0.8	1	1.05	0.031	0.039	0.041
b	0.19		0.30	0.007		0.012
c	0.09		0.20	0.004		0.0089
D	4.9	5	5.1	0.193	0.197	0.201
E	6.2	6.4	6.6	0.244	0.252	0.260
E1	4.3	4.4	4.48	0.169	0.173	0.176
e		0.65 BSC			0.0256 BSC	
K	0°		8°	0°		8°
L1	0.45	0.60	0.75	0.018	0.024	0.030

The figure contains three mechanical drawings of the TSSOP14 package. The top-left drawing is a side view showing dimensions A (total height), A1 (lead height), A2 (lead thickness), b (lead width), e (pitch), and c (lead thickness at the base). The top-right drawing is a perspective view showing dimensions K (lead angle), L (lead length), and E (package width). The bottom drawing is a top-down view showing dimensions D (package length) and E1 (package width), and a circle indicating the PIN 1 identification mark.

## 7 Revision history

Date	Revision	Changes
1-Oct.-2003	1	First release.
2-Jan-2005	2	Modifications on AMR <a href="#">Table 1 on page 4</a> (explanation of $V_{id}$ and $V_i$ limits).
1-Jun-2005	3	ESD protection inserted in <a href="#">Table 1 on page 4</a> .
2-Jan-2006	4	$T_j$ and $R_{thjc}$ parameters added in <a href="#">Table 1. on page 4</a> .
4-Oct-2006	5	Editorial update. <a href="#">Table 3</a> moved to <a href="#">Section 5: Macromodels on page 12</a> .

**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2006 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)