DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF4541B
MSI
Programmable timer

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

DESCRIPTION

The HEF4541B is a programmable timer which consists of a 16-stage binary counter, an integrated oscillator to be used with external timing components, an automatic power-on reset and output control logic. The frequency of the oscillator is determined by the external components R_t and C_t within the frequency range 1 Hz to 100 kHz. This oscillator may be replaced by an external clock signal at input RS, the timer advances on the positive-going transition of RS. A LOW on the auto reset input ($\overline{AR}$) and a LOW on the master reset input (MR) enables the internal power-on reset. A HIGH level at input MR resets the counter independent on all other inputs. Resetting disables the oscillator to provide no active power dissipation.

A HIGH at input $\overline{AR}$ turns off the power-on reset to provide a low quiescent power dissipation of the timer. The 16-stage counter divides the oscillator frequency by 2^8, 2^{10}, 2^{13} or 2^{16} depending on the state of the address inputs (A_0, A_1). The divided oscillator frequency is available at output O. The phase input (PH) features a complementary output signal. If the mode select input (MODE) is LOW or HIGH the timer can be used respectively as a single transition timer or 2^n frequency divider.

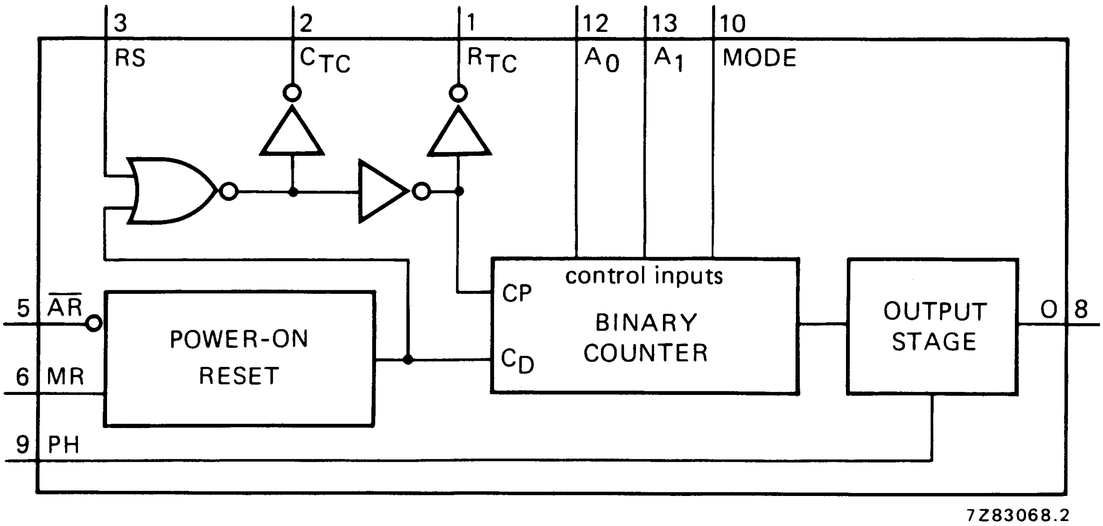


Fig.1 Functional diagram.

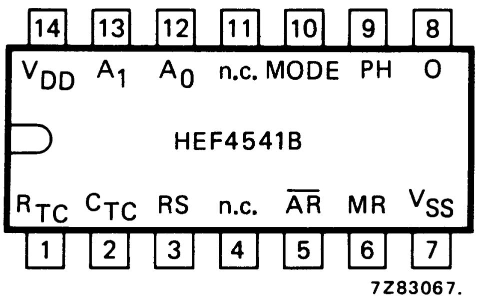


Fig.2 Pinning diagram.

HEF4541BP(N): 14-lead DIL; plastic (SOT27-1)

HEF4541BD(F): 14-lead DIL; ceramic (cerdip) (SOT73)

HEF4541BT(D): 14-lead SO; plastic (SOT108-1)

( ): Package Designator North America

FAMILY DATA, I_{DD} LIMITS category MSI

See Family Specifications

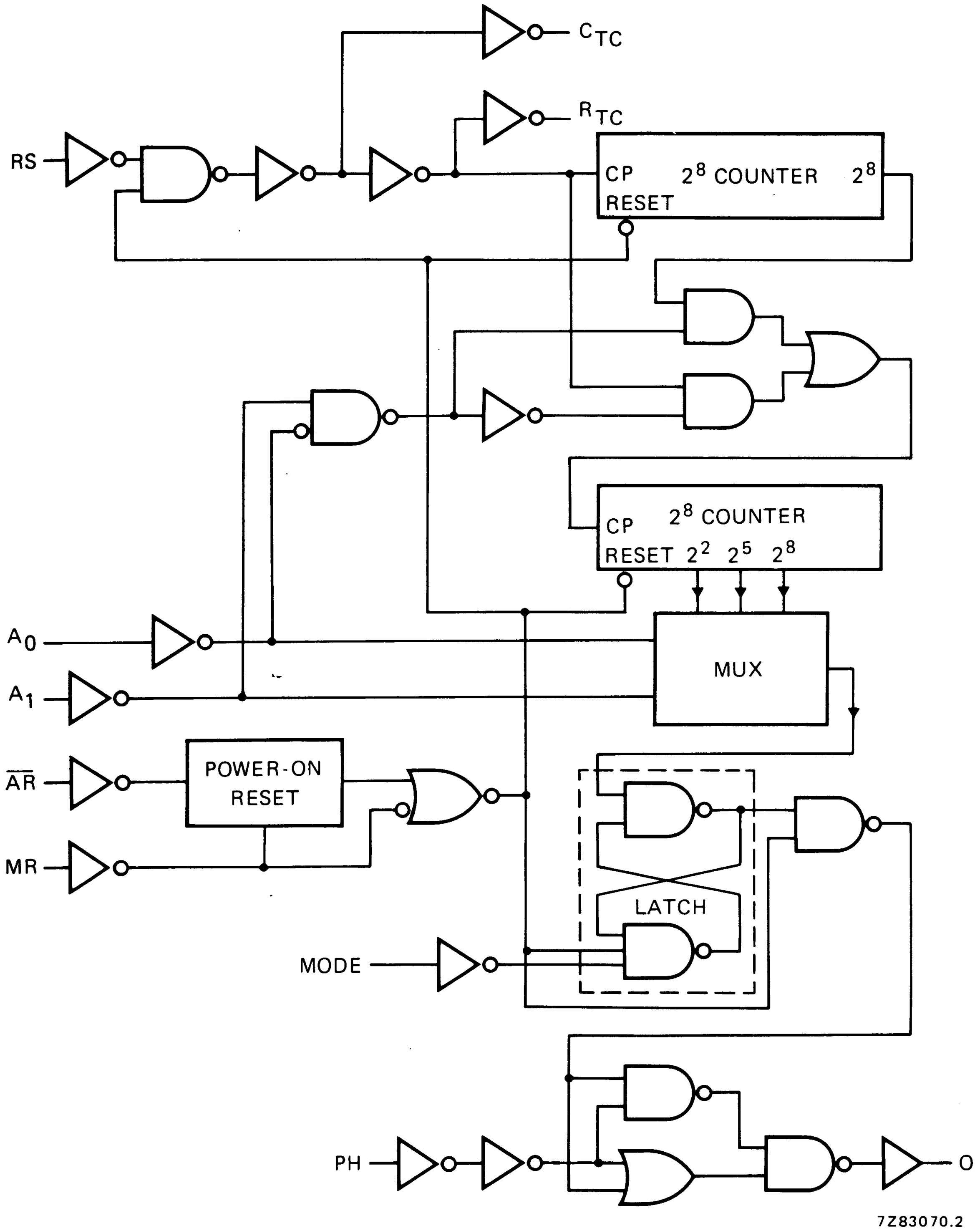


Fig.3 Logic diagram.

PINNING

A_0, A_1	address inputs
MODE	mode select input
$\overline{AR}$	auto reset input
MR	master reset input
PH	phase input
R_{TC}	external resistor connection (R_t)
C_{TC}	external capacitor connection (C_t)
RS	external resistor connection (R_S) or external clock input

FREQUENCY SELECTION TABLE

A_0	A_1	NUMBER OF COUNTER STAGES n	$\frac{f_{osc}}{f_{out}} = 2^n$
L	L	13	8 192
L	H	10	1 024
H	L	8	256
H	H	16	65 536

FUNCTION TABLE

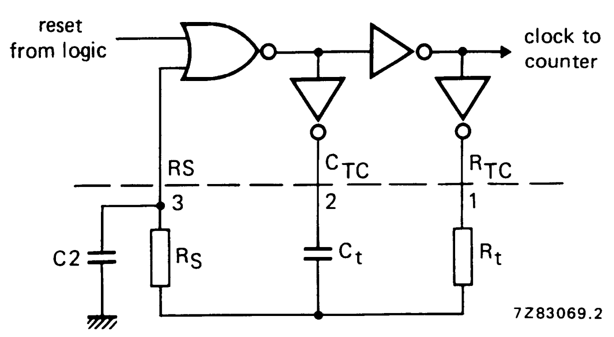
INPUTS				MODE
$\overline{AR}$	MR	PH	MODE	
H	L	X	X	auto reset disabled
L	L	X	X	auto reset enabled (1)
X	H	X	X	master reset active
X	L	X	H	normal operation selected division to output
X	L	X	L	single-cycle mode (2)
X	L	L	X	output initially LOW, after reset
X	L	H	X	output initially HIGH, after reset

Notes

1. For correct power-on reset, the supply voltage should be above 8.5 V. For V_{DD} < 8.5 V, disable the autoreset and connect $\overline{AR}$ to V_{DD}.
2. The timer is initialized on a reset pulse and the output changes state after 2^{n-1} counts and remains in that state (latched). Reset of this latch is obtained by master reset or by a LOW to HIGH transition on the MODE input.

H = HIGH state (the more positive voltage)
L = LOW state (the less positive voltage)
X = state is immaterial

RC oscillator



Typical formula for oscillator frequency:

$$f_{osc} = \frac{1}{2,3 \times R_t \times C_t}$$

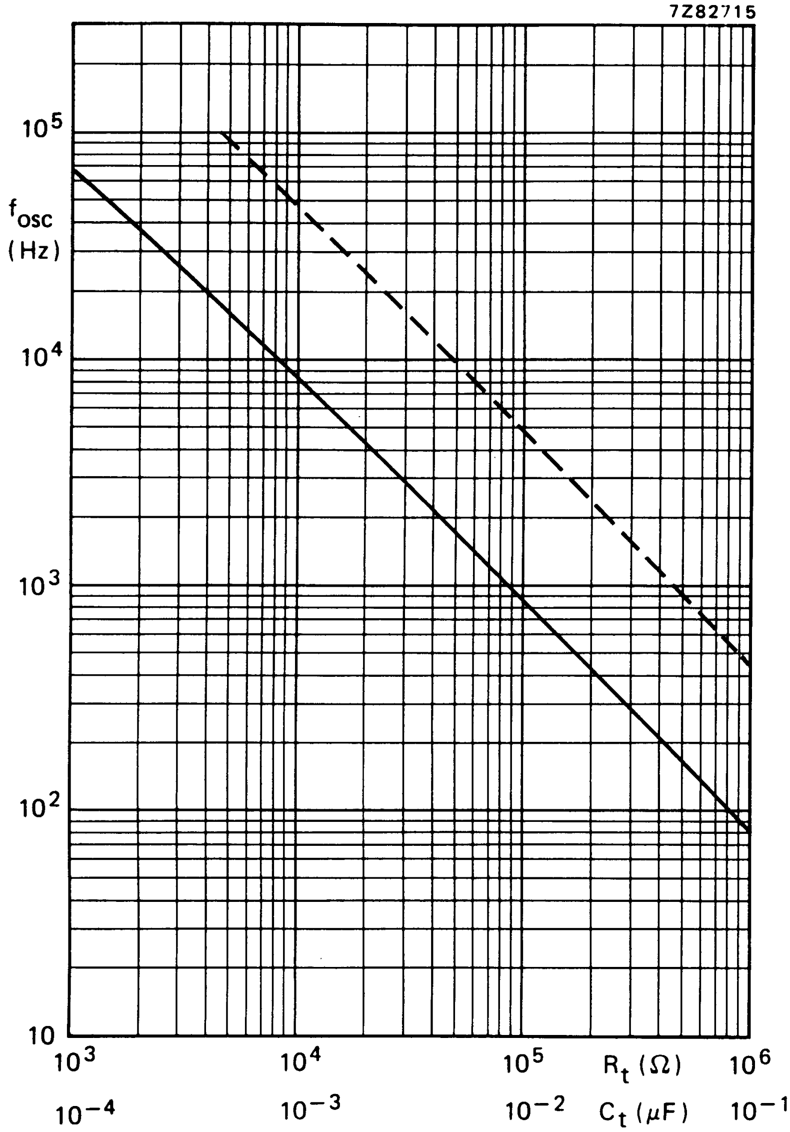
Fig.4 External component connection for RC oscillator; $R_S \approx 2\ R_t$.

Timing component limitations

The oscillator frequency is mainly determined by R_tC_t, provided $R_t << R_S$ and $R_SC2 << R_tC_t$. The function of R_S is to minimize the influence of the forward voltage across the input protection diodes on the frequency. The stray capacitance C2 should be kept as small as possible. In consideration of accuracy, C_t must be larger than the inherent stray capacitance. R_t must be larger than the LOCMOS 'ON' resistance in series with it, which typically is 500 Ω at V_{DD} = 5 V, 300 Ω at V_{DD} = 10 V and 200 Ω at V_{DD} = 15 V.

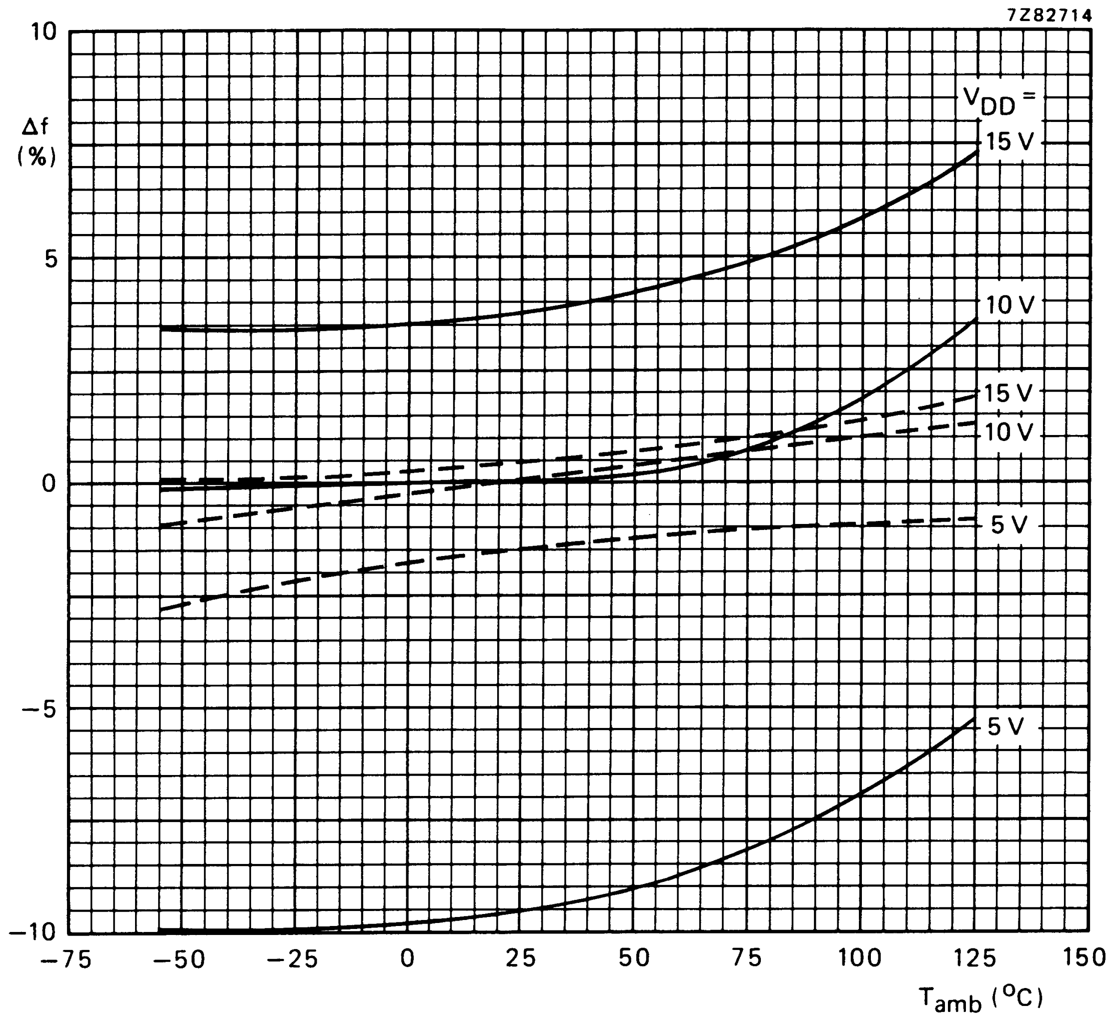
The recommended values for these components to maintain agreement with the typical oscillation formula are:

$C_t \geq 100$ pF, up to any typical value,
10 kΩ $\leq R_t \leq$ 1 MΩ.



—— C_t curve at R_t = 56 kΩ; R_S = 120 kΩ.
– – – R_t curve at C_t = 1 nF; R_S = 2 R_t.

Fig.5 RC oscillator frequency as a function of R_t and C_t at V_{DD} = 5 to 15 V; T_{amb} = 25 °C.



—— R_t = 56 kΩ; C_t = 1 nF; R_S = 0.
– – – R_t = 56 kΩ; C_t = 1 nF; R_S = 120 kΩ.

Fig.6 Frequency deviation (Δf) as a function of ambient temperature; referenced at : f_{osc} at T_{amb} = 25 °C and V_{DD} = 10 V.

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OL} V	V_{OH} V	SYMBOL	T_{amb} (°C) −40 MIN.	MAX.	+ 25 MIN.	TYP.	MAX.	+ 85 MIN.	MAX.	
Supply current	5				–	80	–	20	80	–	230	µA
power-on reset	10			I_D	–	750	–	250	600	–	700	µA
enabled (note)	15				–	1600	–	500	1300	–	1500	µA
Supply voltage for automatic reset initialization (note)				V_{DD}	–	–	8,5	5	–	–	–	V
Output current	5		4,6		0,5	–	0,4	–	–	0,3	–	mA
HIGH; C_{TC}, R_{TC}	10		9,5	$-I_{OH}$	1,4	–	1,2	–	–	0,95	–	mA
	15		13,5		4,8	–	4,0	–	–	3,2	–	mA
	5		2,5	$-I_{OH}$	1,4	–	1,2	–	–	0,95	–	mA
Output current	5	0,4			0,33	–	0,27	–	–	0,20	–	mA
LOW; C_{TC}, R_{TC}	10	0,5		I_{OL}	1,00	–	0,85	–	–	0,68	–	mA
	15	1,5			3,20	–	2,70	–	–	2,30	–	mA

Note

1. All inputs at 0 V or V_{DD}; except input $\overline{AR}$ = input MR = 0 V (power-on reset active).

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; input transition times ≤ 20 ns

	V_{DD} V	TYPICAL FORMULA FOR P (µW)[1]
Dynamic power dissipation	5	$1\,300\ f_i + \sum(f_oC_L) \times V_{DD}^2$
per package	10	$5\,300\ f_i + \sum(f_oC_L) \times V_{DD}^2$
(P)	15	$12\,000\ f_i + \sum(f_oC_L) \times V_{DD}^2$
Total power dissipation	5	$1\,300\ f_{osc} + \sum f_oC_LV_{DD}^2 + 2C_tV_{DD}^2\ f_{osc} + 10\ V_{DD}$
when using the	10	$5\,300\ f_{osc} + \sum f_oC_LV_{DD}^2 + 2C_tV_{DD}^2\ f_{osc} + 100\ V_{DD}$
on-chip oscillator (P)	15	$12\,000\ f_{osc} + \sum f_oC_LV_{DD}^2 + 2C_tV_{DD}^2\ f_{osc} + 400\ V_{DD}$

Notes

1. where:

f_i = input frequency (MHz)

f_o = output frequency (MHz)

C_L = load capacitance (pF)

V_{DD} = supply voltage (V)

C_t = timing capacitance (pF)

f_{osc} = oscillator frequency (MHz)

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
RS → O							
2^8 selected	5			375	750	ns	348 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL};		150	300	ns	139 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t_{PLH}		110	220	ns	102 ns + (0,16 ns/pF) C_L
RS → O							
2^{10} selected	5			425	850	ns	398 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL};		165	330	ns	154 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t_{PLH}		120	240	ns	112 ns + (0,16 ns/pF) C_L
RS → O							
2^{13} selected	5			510	1020	ns	483 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL};		190	380	ns	179 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t_{PLH}		135	270	ns	127 ns + (0,16 ns/pF) C_L
RS → O							
2^{16} selected	5			575	1150	ns	548 ns + (0,55 ns/pF) C_L
HIGH to LOW	10	t_{PHL};		210	420	ns	199 ns + (0,23 ns/pF) C_L
LOW to HIGH	15	t_{PLH}		150	300	ns	142 ns + (0,16 ns/pF) C_L
Minimum clock	5		60	30		ns	
pulse width; LOW	10	t_{WRSL}	30	15		ns	
	15		24	12		ns	
Minimum reset	5		60	30		ns	
pulse width; HIGH	10	t_{WMRH}	30	15		ns	
	15		24	12		ns	
Maximum clock	5		8	16		MHz	
pulse frequency	10	f_{max}	15	30		MHz	
	15		18	36		MHz	
Oscillator frequency	5			90		kHz	R_t = 5 kΩ
	10	f_{osc}		90		kHz	C_t = 1 nF
	15			90		kHz	R_S = 10 kΩ
Oscillator frequency	5			8		kHz	R_t = 56 kΩ
	10	f_{osc}		8		kHz	C_t = 1 nF
	15			8		kHz	R_S = 120 kΩ