

74HC573; 74HCT573

Octal D-type transparent latch; 3-state

Rev. 5 — 15 August 2012

Product data sheet

1. General description

The 74HC573; 74HCT573 is a high-speed Si-gate CMOS device and is pin compatible with Low-power Schottky TTL (LSTTL). It is specified in compliance with JEDEC standard no. 7A.

The 74HC573; 74HCT573 has octal D-type transparent latches featuring separate D-type inputs for each latch and 3-state true outputs for bus-oriented applications. A latch enable (LE) input and an output enable (\overline{OE}) input are common to all latches.

When LE is HIGH, data at the Dn inputs enter the latches. In this condition, the latches are transparent, i.e. a latch output changes state each time its corresponding D input changes.

When LE is LOW the latches store the information that was present at the D-inputs a set-up time preceding the HIGH-to-LOW transition of LE. When \overline{OE} is LOW, the contents of the 8 latches are available at the outputs. When \overline{OE} is HIGH, the outputs go to the high-impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the latches.

The 74HC573; 74HCT573 is functionally identical to:

- 74HC563; 74HCT563, but inverted outputs
- 74HC373; 74HCT373, but different pin arrangement

2. Features and benefits

- Input levels:
 - ◆ For 74HC573: CMOS level
 - ◆ For 74HCT573: TTL level
- Inputs and outputs on opposite sides of package allowing easy interface with microprocessors
- Useful as input or output port for microprocessors and microcomputers
- 3-state non-inverting outputs for bus-oriented applications
- Common 3-state output enable input
- Multiple package options
- ESD protection:
 - ◆ HBM JESD22-A114F exceeds 2 000 V
 - ◆ MM JESD22-A115-A exceeds 200 V
- Specified from $-40\text{ }^{\circ}\text{C}$ to $+85\text{ }^{\circ}\text{C}$ and from $-40\text{ }^{\circ}\text{C}$ to $+125\text{ }^{\circ}\text{C}$



3. Ordering information

Table 1. Ordering information

| Type number | Package | | | |
|-------------------------|-------------------|----------|--|----------|
| | Temperature range | Name | Description | Version |
| 74HC573N 74HCT534N | -40 °C to +125 °C | DIP20 | plastic dual in-line package; 20 leads (300 mil) | SOT146-1 |
| 74HC573D 74HCT573D | -40 °C to +125 °C | SO20 | plastic small outline package; 20 leads; body width 7.5 mm | SOT163-1 |
| 74HC573DB 74HCT573DB | -40 °C to +125 °C | SSOP20 | plastic shrink small outline package; 20 leads; body width 5.3 mm | SOT339-1 |
| 74HC573PW 74HCT573PW | -40 °C to +125 °C | TSSOP20 | plastic thin shrink small outline package; 20 leads; body width 4.4 mm | SOT360-1 |
| 74HC573BQ 74HCT573BQ | -40 °C to +125 °C | DHVQFN20 | plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 × 4.5 × 0.85 mm | SOT764-1 |

4. Functional diagram

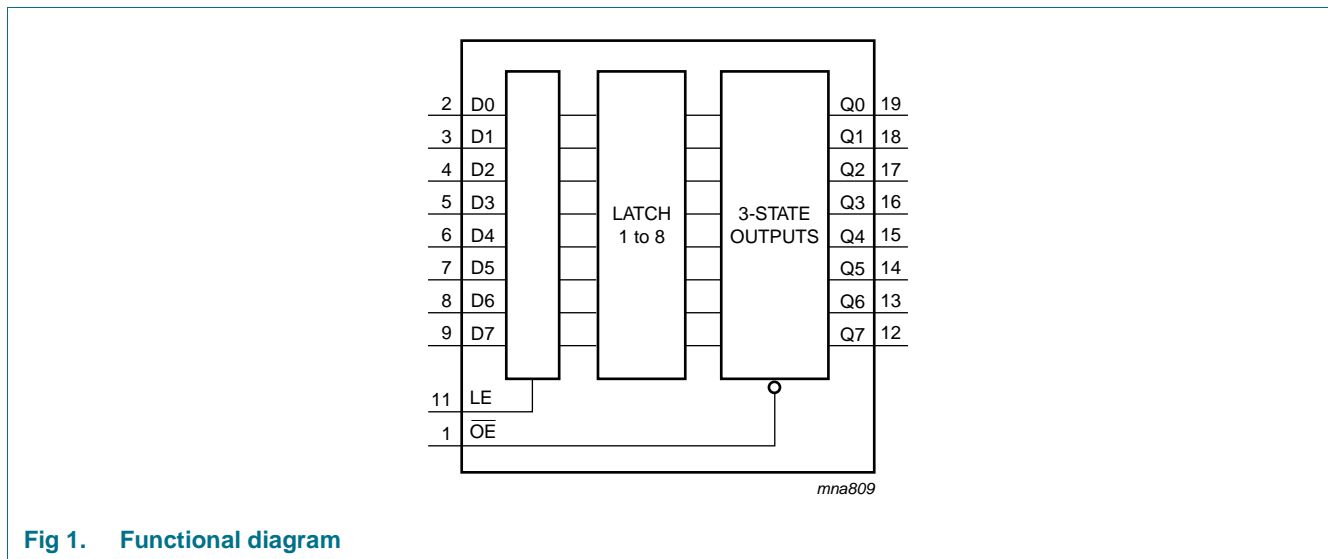


Fig 1. Functional diagram

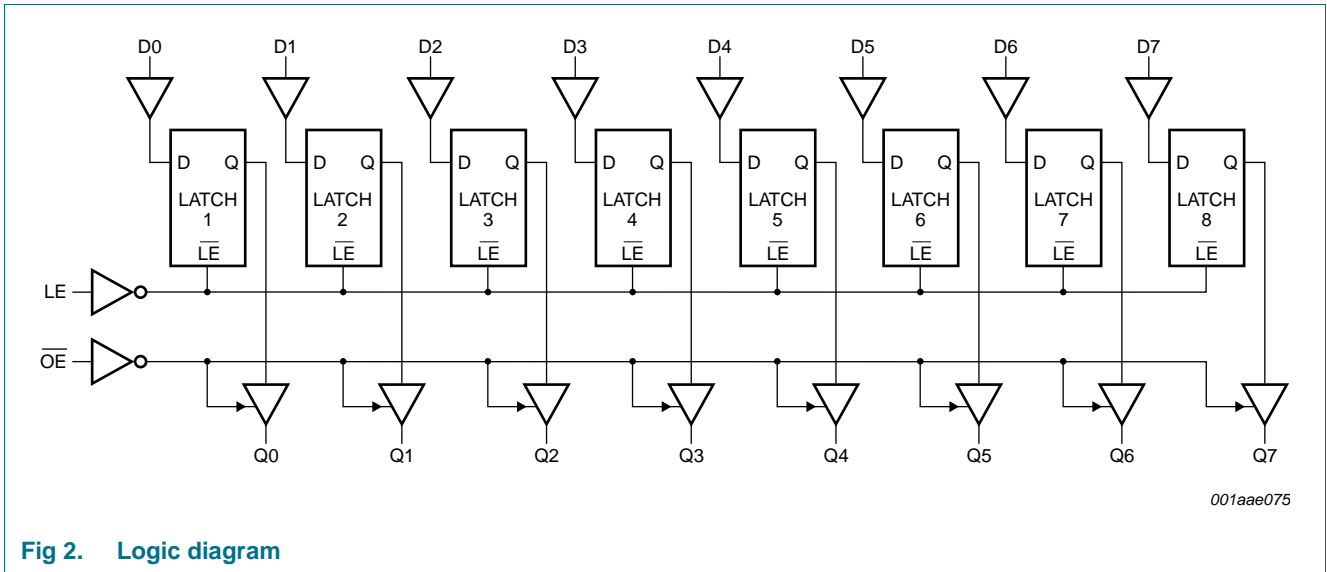


Fig 2. Logic diagram

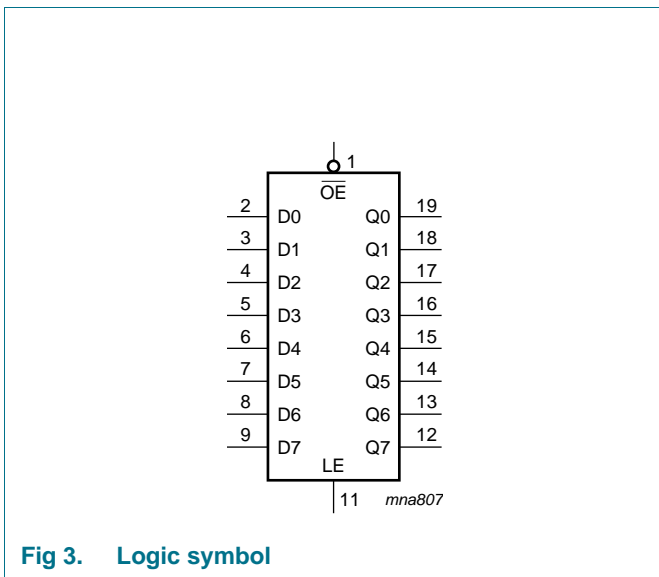


Fig 3. Logic symbol

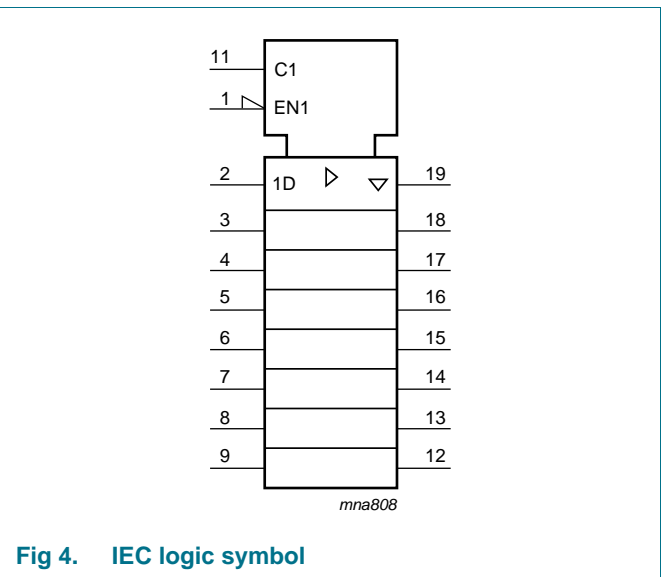
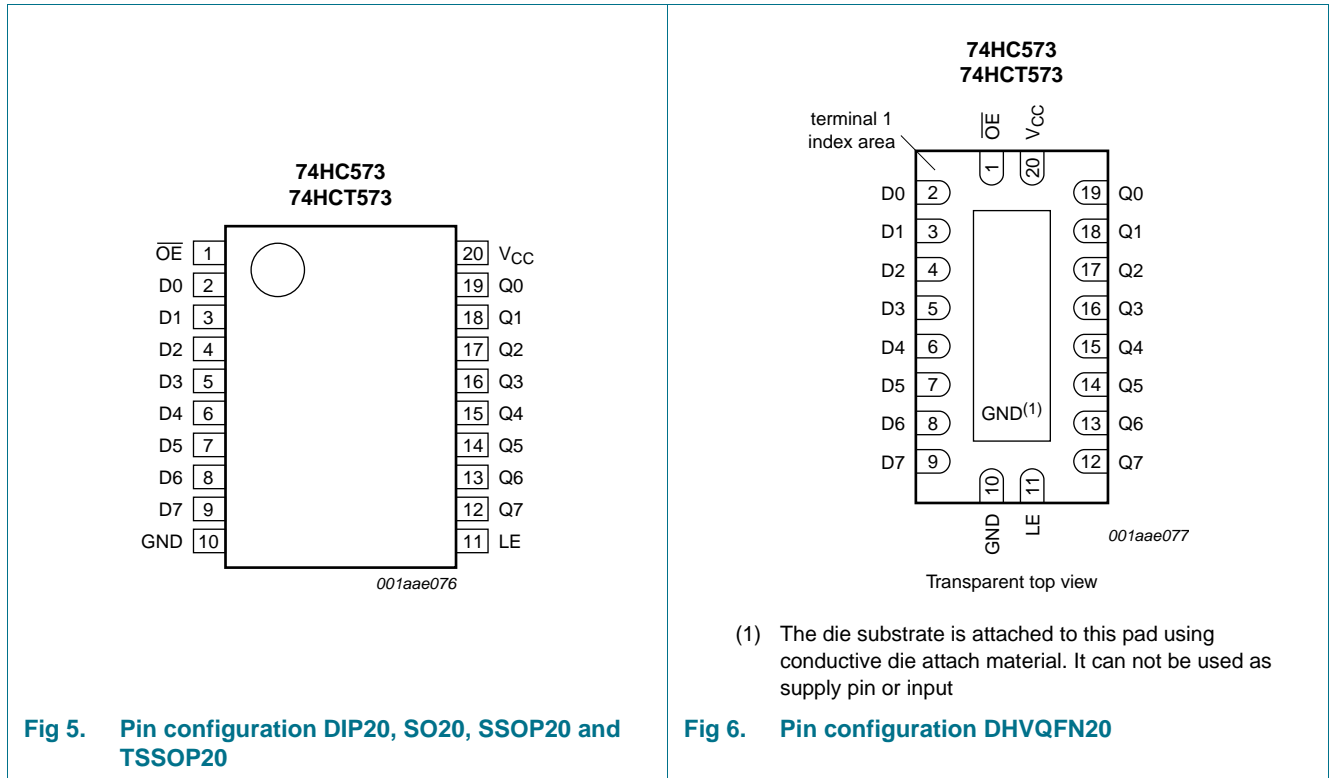


Fig 4. IEC logic symbol

5. Pinning information

5.1 Pinning



5.2 Pin description

Table 2. Pin description

| Symbol | Pin | Description |
|-----------------|--------------------------------|--|
| OE | 1 | 3-state output enable input (active LOW) |
| D[0:7] | 2, 3, 4, 5, 6, 7, 8, 9 | data input |
| GND | 10 | ground (0 V) |
| LE | 11 | latch enable input (active HIGH) |
| Q[0:7] | 19, 18, 17, 16, 15, 14, 13, 12 | 3-state latch output |
| V _{CC} | 20 | supply voltage |

6. Functional description

Table 3. Function table^[1]

| Operating mode | Control | | Input | Internal latches | Output |
|---|---------|----|-------|------------------|--------|
| | OE | LE | Dn | | Qn |
| Enable and read register (transparent mode) | L | H | L | L | L |
| | | | H | H | H |
| Latch and read register | L | L | l | L | L |
| | | | h | H | H |
| Latch register and disable outputs | H | L | l | L | Z |
| | | | h | H | Z |

- [1] H = HIGH voltage level;
h = HIGH voltage level one set-up time prior to the HIGH-to-LOW LE transition;
L = LOW voltage level;
l = LOW voltage level one set-up time prior to the HIGH-to-LOW LE transition;
Z = high-impedance OFF-state.

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134). Voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | Min | Max | Unit |
|-----------|-------------------------|--|------------------|----------|------|
| V_{CC} | supply voltage | | -0.5 | +7 | V |
| I_{IK} | input clamping current | $V_I < -0.5\text{ V}$ or $V_I > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_{OK} | output clamping current | $V_O < -0.5\text{ V}$ or $V_O > V_{CC} + 0.5\text{ V}$ | - | ± 20 | mA |
| I_O | output current | $V_O = -0.5\text{ V}$ to $(V_{CC} + 0.5\text{ V})$ | - | ± 35 | mA |
| I_{CC} | supply current | | - | +70 | mA |
| I_{GND} | ground current | | - | -70 | mA |
| T_{stg} | storage temperature | | -65 | +150 | °C |
| P_{tot} | total power dissipation | DIP20 package | ^[1] - | 750 | mW |
| | | SO20, SSOP20, TSSOP20 and DHVQFN20 packages | ^[2] - | 500 | mW |

- [1] For DIP20 package: P_{tot} derates linearly with 12 mW/K above 70 °C.
[2] For SO20: P_{tot} derates linearly with 8 mW/K above 70 °C.
For SSOP20 and TSSOP20 packages: P_{tot} derates linearly with 5.5 mW/K above 60 °C.
For DHVQFN20 package: P_{tot} derates linearly with 4.5 mW/K above 60 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Voltages are referenced to GND (ground = 0 V)

| Symbol | Parameter | Conditions | 74HC573 | | | 74HCT573 | | | Unit |
|------------------|-------------------------------------|-------------------------|---------|------|-----------------|----------|------|-----------------|------|
| | | | Min | Typ | Max | Min | Typ | Max | |
| V _{CC} | supply voltage | | 2.0 | 5.0 | 6.0 | 4.5 | 5.0 | 5.5 | V |
| V _I | input voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| V _O | output voltage | | 0 | - | V _{CC} | 0 | - | V _{CC} | V |
| T _{amb} | ambient temperature | | -40 | +25 | +125 | -40 | +25 | +125 | °C |
| Δt/ΔV | input transition rise and fall rate | V _{CC} = 2.0 V | - | - | 625 | - | - | - | ns/V |
| | | V _{CC} = 4.5 V | - | 1.67 | 139 | - | 1.67 | 139 | ns/V |
| | | V _{CC} = 6.0 V | - | - | 83 | - | - | - | ns/V |

9. Static characteristics

Table 6. Static characteristics

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-----------------|---------------------------|--|-------|------|------|------------------|------|-------------------|-------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| 74HC573 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 2.0 V | 1.5 | 1.2 | - | 1.5 | - | 1.5 | - | V |
| | | V _{CC} = 4.5 V | 3.15 | 2.4 | - | 3.15 | - | 3.15 | - | V |
| | | V _{CC} = 6.0 V | 4.2 | 3.2 | - | 4.2 | - | 4.2 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 2.0 V | - | 0.8 | 0.5 | - | 0.5 | - | 0.5 | V |
| | | V _{CC} = 4.5 V | - | 2.1 | 1.35 | - | 1.35 | - | 1.35 | V |
| | | V _{CC} = 6.0 V | - | 2.8 | 1.8 | - | 1.8 | - | 1.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = -20 μA; V _{CC} = 2.0 V | 1.9 | 2.0 | - | 1.9 | - | 1.9 | - | V |
| | | I _O = -20 μA; V _{CC} = 4.5 V | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -20 μA; V _{CC} = 6.0 V | 5.9 | 6.0 | - | 5.9 | - | 5.9 | - | V |
| | | I _O = -6.0 mA; V _{CC} = 4.5 V | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} | | | | | | | | |
| | | I _O = 20 μA; V _{CC} = 2.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 4.5 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 20 μA; V _{CC} = 6.0 V | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA; V _{CC} = 4.5 V | - | 0.15 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| | | V _I = V _{IH} or V _{IL} ; V _O = V _{CC} or GND; V _{CC} = 6.0 V | - | - | ±0.5 | - | ±5.0 | - | ±10.0 | μA |

Table 6. Static characteristics ...continued

At recommended operating conditions; voltages are referenced to GND (ground = 0 V).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|------------------|---------------------------|--|-------|------|------|------------------|------|-------------------|------|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 6.0 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF |
| 74HCT573 | | | | | | | | | | |
| V _{IH} | HIGH-level input voltage | V _{CC} = 4.5 V to 5.5 V | 2.0 | 1.6 | - | 2.0 | - | 2.0 | - | V |
| V _{IL} | LOW-level input voltage | V _{CC} = 4.5 V to 5.5 V | - | 1.2 | 0.8 | - | 0.8 | - | 0.8 | V |
| V _{OH} | HIGH-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = -20 μA | 4.4 | 4.5 | - | 4.4 | - | 4.4 | - | V |
| | | I _O = -6 mA | 3.98 | 4.32 | - | 3.84 | - | 3.7 | - | V |
| V _{OL} | LOW-level output voltage | V _I = V _{IH} or V _{IL} ; V _{CC} = 4.5 V | | | | | | | | |
| | | I _O = 20 μA | - | 0 | 0.1 | - | 0.1 | - | 0.1 | V |
| | | I _O = 6.0 mA | - | 0.16 | 0.26 | - | 0.33 | - | 0.4 | V |
| I _I | input leakage current | V _I = V _{CC} or GND; V _{CC} = 5.5 V | - | - | ±0.1 | - | ±1.0 | - | ±1.0 | μA |
| I _{OZ} | OFF-state output current | V _I = V _{IH} or V _{IL} ; V _{CC} = 5.5 V; V _O = V _{CC} or GND per input pin; other inputs at V _{CC} or GND; I _O = 0 A | - | - | ±0.5 | - | ±5.0 | - | ±10 | μA |
| I _{CC} | supply current | V _I = V _{CC} or GND; I _O = 0 A; V _{CC} = 5.5 V | - | - | 8.0 | - | 80 | - | 160 | μA |
| ΔI _{CC} | additional supply current | V _I = V _{CC} - 2.1 V; other inputs at V _{CC} or GND; V _{CC} = 4.5 V to 5.5 V; I _O = 0 A | | | | | | | | |
| | | per input pin; Dn inputs | - | 35 | 126 | - | 158 | - | 172 | μA |
| | | per input pin; LE input | - | 65 | 234 | - | 293 | - | 319 | μA |
| | | per input pin; \overline{OE} input | - | 125 | 450 | - | 563 | - | 613 | μA |
| C _I | input capacitance | | - | 3.5 | - | | | | | pF |

10. Dynamic characteristics

Table 7. Dynamic characteristics

Voltages are referenced to GND (ground = 0 V); $C_L = 50$ pF unless otherwise specified; for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|-------------------------|-------------------------------|---|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| For type 74HC573 | | | | | | | | | | |
| t_{pd} | propagation delay | Dn to Qn; see Figure 7 [1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 47 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | 17 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 14 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V | - | 14 | 26 | - | 33 | - | 38 | ns |
| t_{pd} | propagation delay | LE to Qn; see Figure 8 [1] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 50 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | 18 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 5$ V; $C_L = 15$ pF | - | 15 | - | - | - | - | - | ns |
| | | $V_{CC} = 6.0$ V | - | 14 | 26 | - | 33 | - | 38 | ns |
| t_{en} | enable time | \overline{OE} to Qn; see Figure 9 [2] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 44 | 140 | - | 175 | - | 210 | ns |
| | | $V_{CC} = 4.5$ V | - | 16 | 28 | - | 35 | - | 42 | ns |
| | | $V_{CC} = 6.0$ V | - | 13 | 24 | - | 30 | - | 36 | ns |
| t_{dis} | disable time | \overline{OE} to Qn; see Figure 9 [3] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 55 | 150 | - | 190 | - | 225 | ns |
| | | $V_{CC} = 4.5$ V | - | 20 | 30 | - | 38 | - | 45 | ns |
| | | $V_{CC} = 6.0$ V | - | 16 | 26 | - | 33 | - | 38 | ns |
| t_t | transition time | Qn; see Figure 7 [4] | | | | | | | | |
| | | $V_{CC} = 2.0$ V | - | 14 | 60 | - | 75 | - | 90 | ns |
| | | $V_{CC} = 4.5$ V | - | 5 | 12 | - | 15 | - | 18 | ns |
| | | $V_{CC} = 6.0$ V | - | 4 | 10 | - | 13 | - | 15 | ns |
| t_W | pulse width | LE HIGH; see Figure 8 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 80 | 14 | - | 100 | - | 120 | - | ns |
| | | $V_{CC} = 4.5$ V | 16 | 5 | - | 20 | - | 24 | - | ns |
| | | $V_{CC} = 6.0$ V | 14 | 4 | - | 17 | - | 20 | - | ns |
| t_{su} | set-up time | Dn to LE; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 50 | 11 | - | 65 | - | 75 | - | ns |
| | | $V_{CC} = 4.5$ V | 10 | 4 | - | 13 | - | 15 | - | ns |
| | | $V_{CC} = 6.0$ V | 9 | 3 | - | 11 | - | 13 | - | ns |
| t_h | hold time | Dn to LE; see Figure 10 | | | | | | | | |
| | | $V_{CC} = 2.0$ V | 5 | 3 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 4.5$ V | 5 | 1 | - | 5 | - | 5 | - | ns |
| | | $V_{CC} = 6.0$ V | 5 | 1 | - | 5 | - | 5 | - | ns |
| C_{PD} | power dissipation capacitance | $C_L = 50$ pF; $f = 1$ MHz; $V_1 = \text{GND to } V_{CC}$ [5] | - | 26 | - | - | - | - | - | pF |

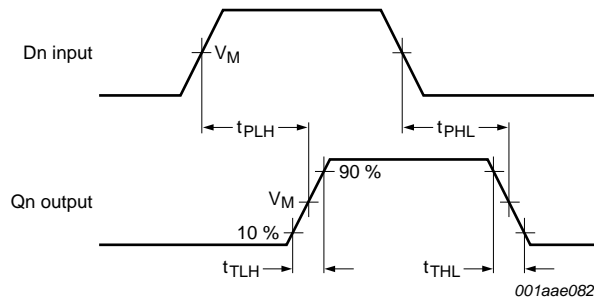
Table 7. Dynamic characteristics ...continued

Voltages are referenced to GND (ground = 0 V); C_L = 50 pF unless otherwise specified; for test circuit see [Figure 11](#).

| Symbol | Parameter | Conditions | 25 °C | | | -40 °C to +85 °C | | -40 °C to +125 °C | | Unit |
|--------------------------|-------------------------------|--|-------|-----|-----|------------------|-----|-------------------|-----|------|
| | | | Min | Typ | Max | Min | Max | Min | Max | |
| For type 74HCT573 | | | | | | | | | | |
| t _{pd} | propagation delay | Dn to Qn; see Figure 7 [1] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 20 | 35 | - | 44 | - | 53 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 17 | - | - | - | - | - | ns |
| t _{pd} | propagation delay | LE to Qn; see Figure 8 [1] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 18 | 35 | - | 44 | - | 53 | ns |
| | | V _{CC} = 5 V; C _L = 15 pF | - | 15 | - | - | - | - | - | ns |
| t _{en} | enable time | \overline{OE} to Qn; see Figure 9 [2] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 17 | 30 | - | 38 | - | 45 | ns |
| t _{dis} | disable time | \overline{OE} to Qn; see Figure 9 [3] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 18 | 30 | - | 38 | - | 45 | ns |
| t _t | transition time | Qn; see Figure 7 [4] | | | | | | | | |
| | | V _{CC} = 4.5 V | - | 5 | 12 | - | 15 | - | 18 | ns |
| t _W | pulse width | LE HIGH; see Figure 8 | | | | | | | | |
| | | V _{CC} = 4.5 V | 16 | 5 | - | 20 | - | 24 | - | ns |
| t _{su} | set-up time | Dn to LE; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 13 | 7 | - | 16 | - | 20 | - | ns |
| t _h | hold time | Dn to LE; see Figure 10 | | | | | | | | |
| | | V _{CC} = 4.5 V | 9 | 4 | - | 11 | - | 15 | - | ns |
| C _{PD} | power dissipation capacitance | C _L = 50 pF; f = 1 MHz; V _I = GND to V _{CC} | [5] | - | 26 | - | - | - | - | pF |

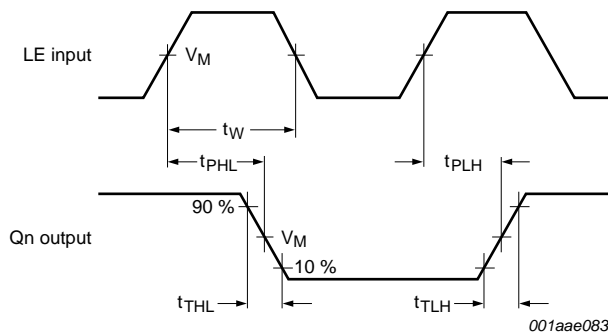
- [1] t_{pd} is the same as t_{PLH} and t_{PHL}.
- [2] t_{en} is the same as t_{PZH} and t_{PZL}.
- [3] t_{dis} is the same as t_{PLZ} and t_{PHZ}.
- [4] t_t is the same as t_{THL} and t_{TLH}.
- [5] C_{PD} is used to determine the dynamic power dissipation (P_D in μW).
 $P_D = C_{PD} \times V_{CC}^2 \times f_i \times N + \sum(C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz;
 f_o = output frequency in MHz;
 C_L = output load capacitance in pF;
 V_{CC} = supply voltage in V;
 N = number of inputs switching;
 $\sum(C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.

11. Waveforms



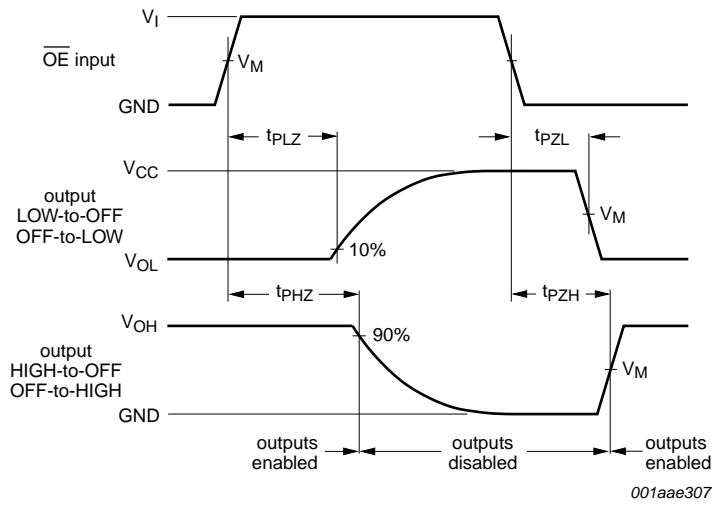
Measurement points are given in [Table 8](#).

Fig 7. Propagation delay data input (Dn) to output (Qn) and output transition time



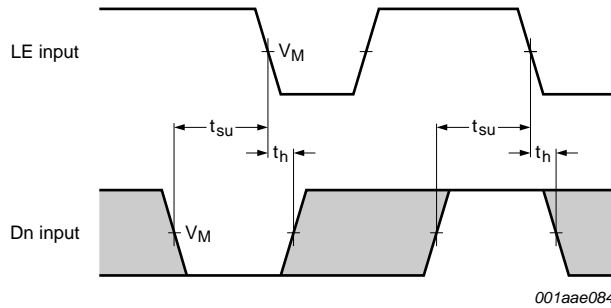
Measurement points are given in [Table 8](#).

Fig 8. Pulse width latch enable input (LE), propagation delay latch enable input (LE) to output (Qn) and output transition time



Measurement points are given in [Table 8](#).
 V_{OL} and V_{OH} are typical voltage output levels that occur with the output load.

Fig 9. Enable and disable times



Measurement points are given in [Table 8](#).
 The shaded areas indicate when the input is permitted to change for predictable output performance.

Fig 10. Set-up and hold times for data input (Dn) to latch input (LE)

Table 8. Measurement points

| Type | Input | Output |
|----------|-------------|-------------|
| | V_M | V_M |
| 74HC573 | $0.5V_{CC}$ | $0.5V_{CC}$ |
| 74HCT573 | 1.3 V | 1.3 V |

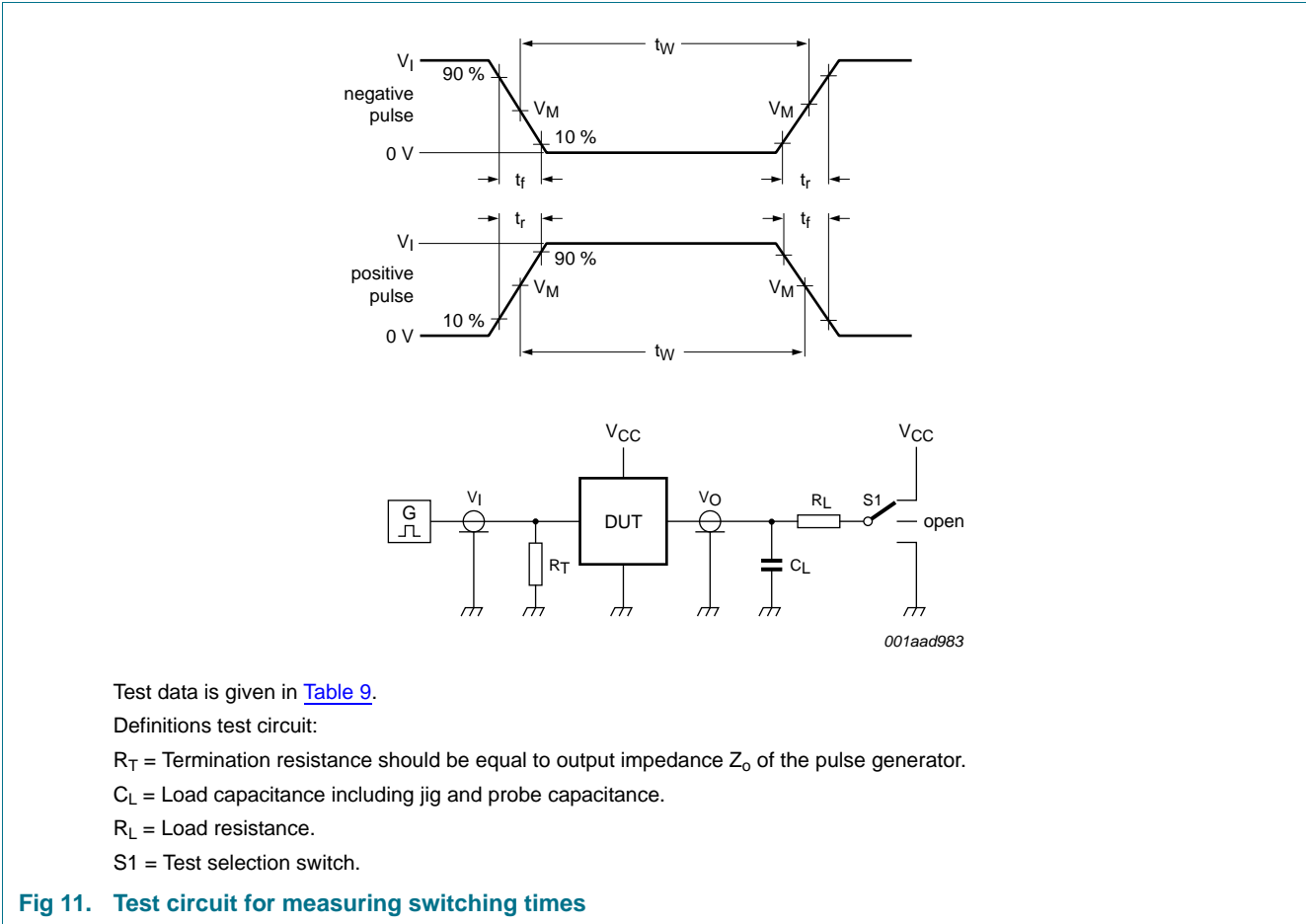


Table 9. Test data

| Type | Input | | Load | | S1 position | | |
|----------|----------|------------|--------------|--------------|--------------------|--------------------|--------------------|
| | V_I | t_r, t_f | C_L | R_L | t_{PHL}, t_{PLH} | t_{PZH}, t_{PHZ} | t_{PZL}, t_{PLZ} |
| 74HC573 | V_{CC} | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |
| 74HCT573 | 3 V | 6 ns | 15 pF, 50 pF | 1 k Ω | open | GND | V_{CC} |

12. Package outline

DIP20: plastic dual in-line package; 20 leads (300 mil)

SOT146-1

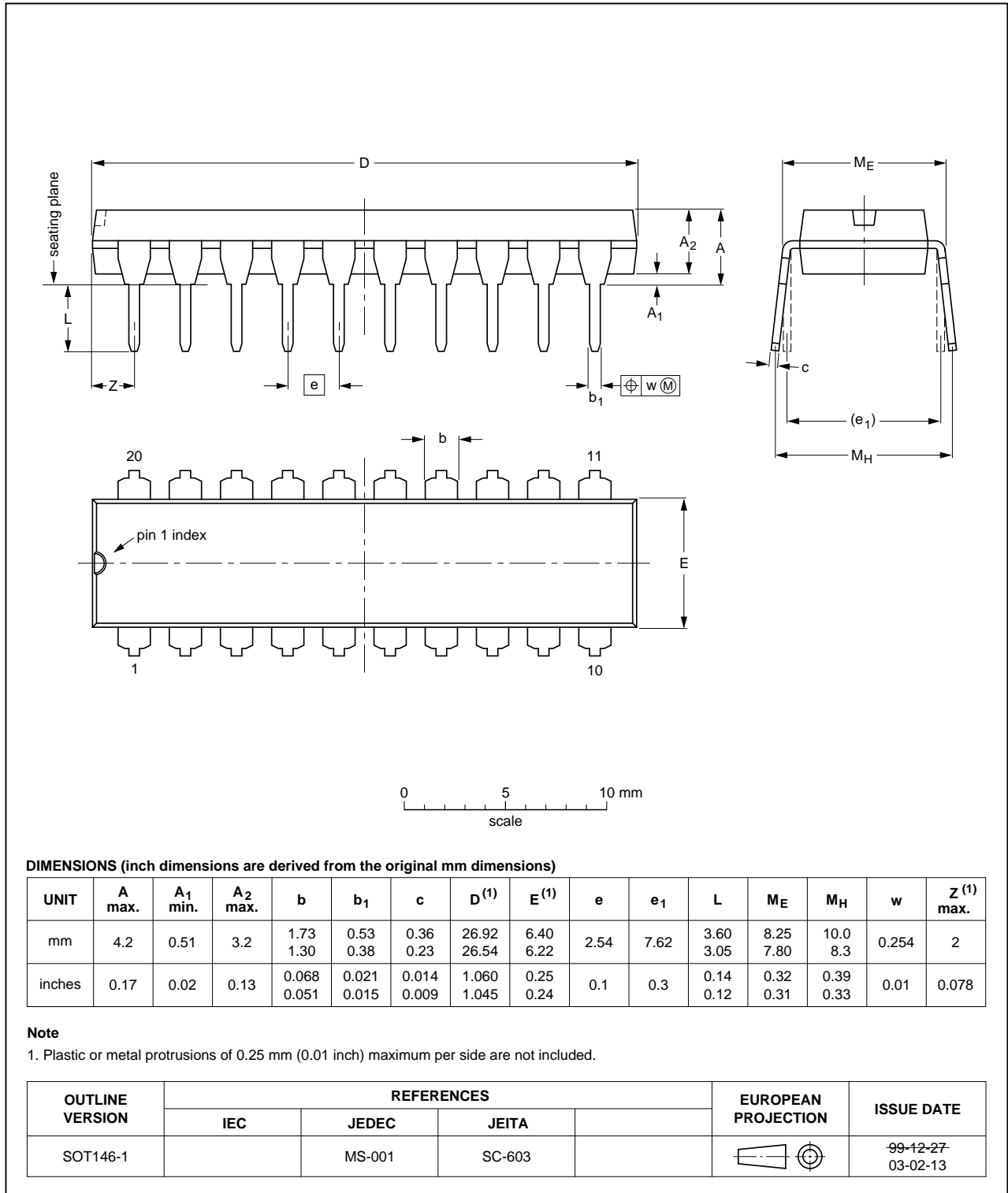


Fig 12. Package outline SOT146-1 (DIP20)

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1

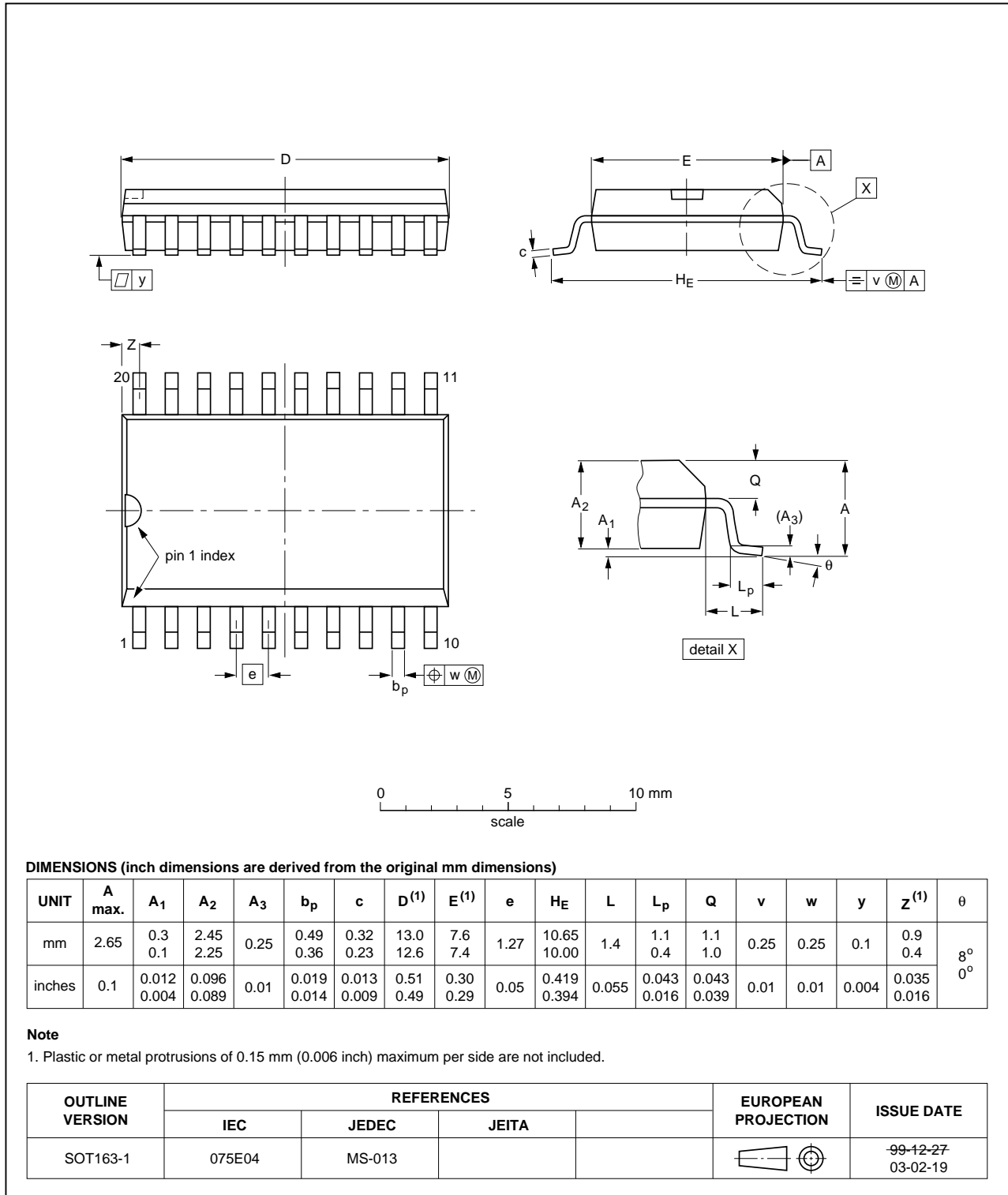


Fig 13. Package outline SOT163-1 (SO20)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1

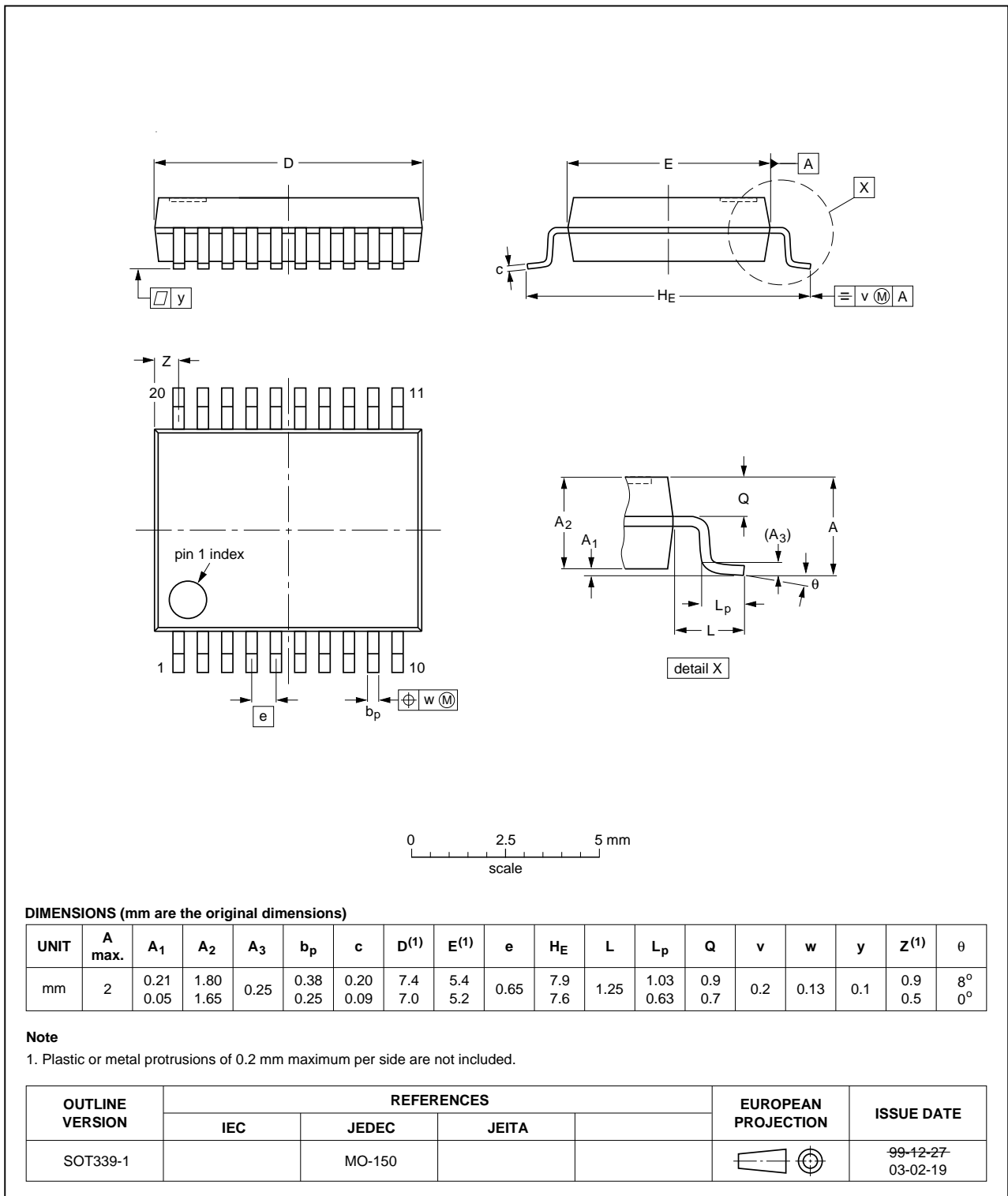


Fig 14. Package outline SOT339-1 (SSOP20)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1

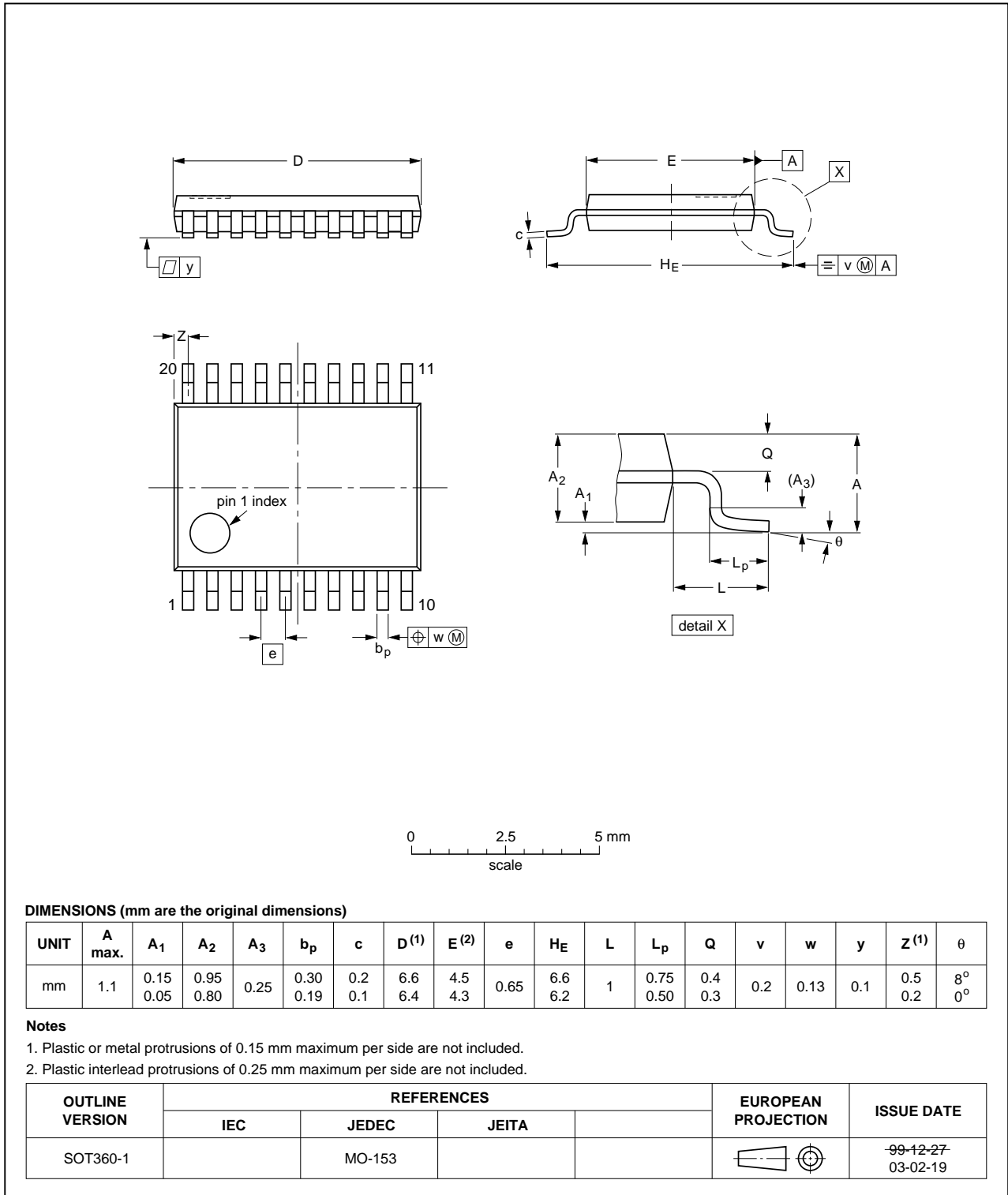


Fig 15. Package outline SOT360-1 (TSSOP20)

DHVQFN20: plastic dual in-line compatible thermal enhanced very thin quad flat package; no leads; 20 terminals; body 2.5 x 4.5 x 0.85 mm

SOT764-1

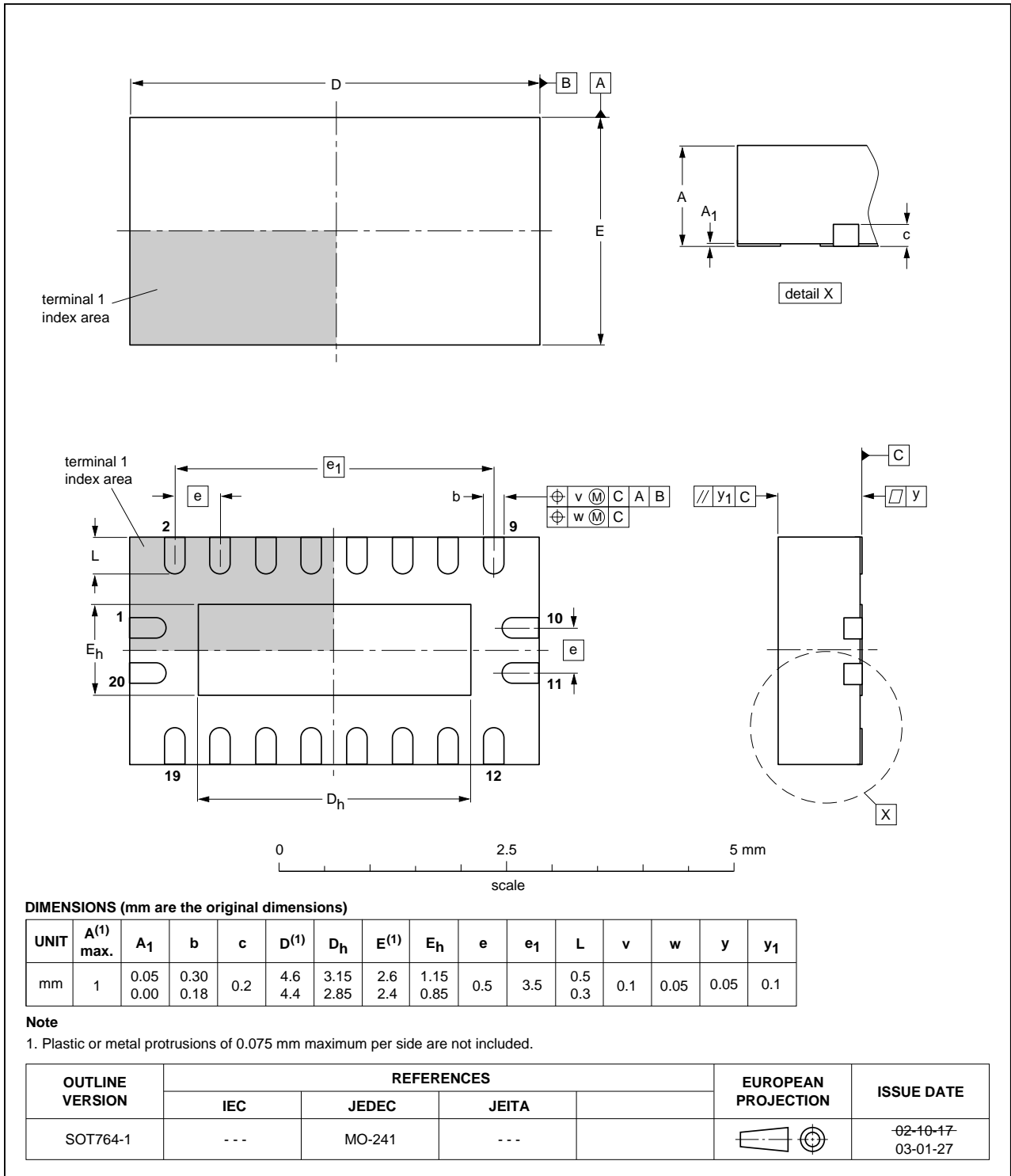


Fig 16. Package outline SOT764-1 (DHVQFN20)

13. Abbreviations

Table 10. Abbreviations

| Acronym | Description |
|---------|---|
| CMOS | Complementary Metal Oxide Semiconductor |
| ESD | ElectroStatic Discharge |
| HBM | Human Body Model |
| MM | Machine Model |
| TTL | Transistor-Transistor Logic |

14. Revision history

Table 11. Revision history

| Document ID | Release date | Data sheet status | Change notice | Supersedes |
|---------------------|---|-----------------------|---------------|---------------------|
| 74HC_HCT573 v.5 | 20120815 | Product data sheet | - | 74HC_HCT573 v.3 |
| Modifications: | <ul style="list-style-type: none"> Alternative descriptive title corrected (errata). | | | |
| 74HC_HCT573 v.4 | 20120806 | Product data sheet | - | 74HC_HCT573 v.3 |
| Modifications: | <ul style="list-style-type: none"> The format of this data sheet has been redesigned to comply with the new identity guidelines of NXP Semiconductors. Legal texts have been adapted to the new company name where appropriate. | | | |
| 74HC_HCT573 v.3 | 20060117 | Product data sheet | - | 74HC_HCT573_CNV v.2 |
| 74HC_HCT573_CNV v.2 | 19901201 | Product specification | - | - |

15. Legal information

15.1 Data sheet status

| Document status ^{[1][2]} | Product status ^[3] | Definition |
|-----------------------------------|-------------------------------|---|
| Objective [short] data sheet | Development | This document contains data from the objective specification for product development. |
| Preliminary [short] data sheet | Qualification | This document contains data from the preliminary specification. |
| Product [short] data sheet | Production | This document contains the product specification. |

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL <http://www.nxp.com>.

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